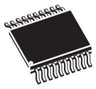
STM32U031x4/6/8

Datasheet

Ultra-low-power Arm® Cortex®-M0+ 32-bit MCU, up to 64-Kbyte flash memory, 12-Kbyte SRAM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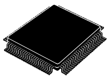
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LQFP64
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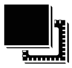
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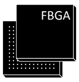

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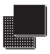

WLCSP27
(2.55 x 2.34 mm)

Product summary	
STM32U031x4	STM32U031F4, STM32U031K4
STM32U031x6	STM32U031F6, STM32U031K6, STM32U031C6, STM32U031R6, STM32U031G6
STM32U031x8	STM32U031F8, STM32U031K8, STM32U031C8, STM32U031R8, STM32U031G8

Product label

SUSTAINABLE TECHNOLOGY

Features

Includes ST state-of-the-art patented technology.

Ultra-low-power features (ultra-low-power devices)

- 1.71 V to 3.6 V power supply
- -40 °C to 85/125 °C temperature range
- VBAT mode: 130 nA (with RTC and 9 x 32-bit backup registers)
- Shutdown mode (4 wake-up pins): 16 nA
- Standby mode (4 wake-up pins): 160 nA with RTC, 30 nA without RTC
- Stop 2 mode: 630 nA with RTC, 515 nA without RTC
- Run mode (LDO mode): 52 µA/MHz
- Batch acquisition mode (BAM)
- 4 µs wake-up from Stop mode
- Brownout reset (BOR)

Core

- 32-bit Arm® Cortex®-M0+ CPU, frequency up to 56 MHz

ART Accelerator

- 1-Kbyte instruction cache allowing 0-wait-state execution from flash memory

Benchmarks

- 1.13 DMIPS/MHz (Drystone 2.1)
- 134 CoreMark® (2.4 CoreMark/MHz at 56 MHz)
- 430 ULPMark™-CP
- 167 ULPMark™-PP
- 20.3 ULPMark™-CM

Memories

- Up to 64-Kbyte single bank flash memory, proprietary code readout protection
- 12-Kbyte SRAM with hardware parity check

Rich analog peripherals (independent supply)

- 1x 12-bit ADC (0.4 µs conversion time), up to 16-bit with hardware oversampling
- 1x 12-bit DAC output channel, low-power sample and hold
- 1x general-purpose operational amplifier with built-in PGA (variable gain up to 16)
- 1x ultra-low-power comparator

General-purpose inputs/outputs

- Up to 53 fast I/Os, most of them 5 V-tolerant

16 communication interfaces

- 6x USARTs/LPUARTs (SPI, ISO 7816, LIN, IrDA, modem)
- 3x I2C interfaces supporting Fast-mode and Fast-mode Plus (up to 1 Mbit/s)
- 2x SPIs, plus 4x USARTs in SPI mode
- IRTIM (Infrared interface)

Security

- Customer code protection
- Robust read out protection (RDP): 3 protection level states and password-based regression (128-bit PSWD)
- Hardware protection feature (HDP)
- Secure boot
- True random number generation, candidate for NIST SP 800-90B certification
- Candidate for Arm® PSA level 1 and SESIP level 3 certifications
- 5 passive anti-tamper pins
- 96-bit unique ID

Clock management

- 4 to 48 MHz crystal oscillator
- 32 kHz crystal oscillator for RTC (LSE)
- Internal 16 MHz factory-trimmed RC (±1%)
- Internal low-power 32 kHz RC (±5%)
- Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
- PLL for system clock, ADC

9 timers, RTC, and 2 watchdogs

- 1x 16-bit advanced motor-control, 1x 32-bit and 3x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- RTC with hardware calendar, alarms and calibration

CRC calculation unit

Up to 18 capacitive sensing channels

- Supporting touchkey, linear and rotary touch sensors

7-channel DMA controller

- Flexible mapping (DMAMUX)

Debug

- Development support: serial wire debug (SWD)

All packages are ECOPACK2 compliant.

1 Introduction

This document provides information on STM32U031x4/6/8 devices, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging and ordering information.

It must be read in conjunction with the STM32U031x4/6/8 reference manual (RM0503).

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32U031x4/6/8 errata sheet (ES0603).

For information on the Arm® Cortex®-M0+ core, refer to the Cortex-M0+ Technical Reference Manual, available from the www.arm.com website.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32U031x4/6/8 devices are ultra-low-power microcontrollers based on the high-performance Arm® Cortex®-M0+ 32-bit RISC core operating at a frequency of up to 56 MHz.

The STM32U031x4/6/8 devices embed high-speed memories (up to 64-Kbyte flash memory and 12-Kbyte SRAM with hardware parity check), and an extensive range of enhanced I/Os and peripherals connected to APB and AHB buses, and a 32-bit multi-AHB bus matrix.

They also embed protection mechanisms for embedded flash memory and SRAM, such as readout protection and write protection.

The STM32U031x4/6/8 devices offer a 12-bit ADC, a 12-bit DAC, an embedded rail-to-rail analog comparator, one operational amplifier, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, three general-purpose 16-bit timers, and two 16-bit low-power timers

The devices also embed up to 21 capacitive sensing channels.

They also feature standard and advanced communication interfaces, namely three I2Cs, two SPIs, four USARTs and two low-power UARTs.

The STM32U031x4/6/8 operate in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V V_{DD} power supply using an internal LDO regulator. A comprehensive set of power-saving modes makes possible the design of low-power applications.

Independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMP and comparator, as well as VBAT input allowing the backup of the RTC and backup registers.

The STM32U031x4/6/8 offer eight packages from 20 to 64 pins.

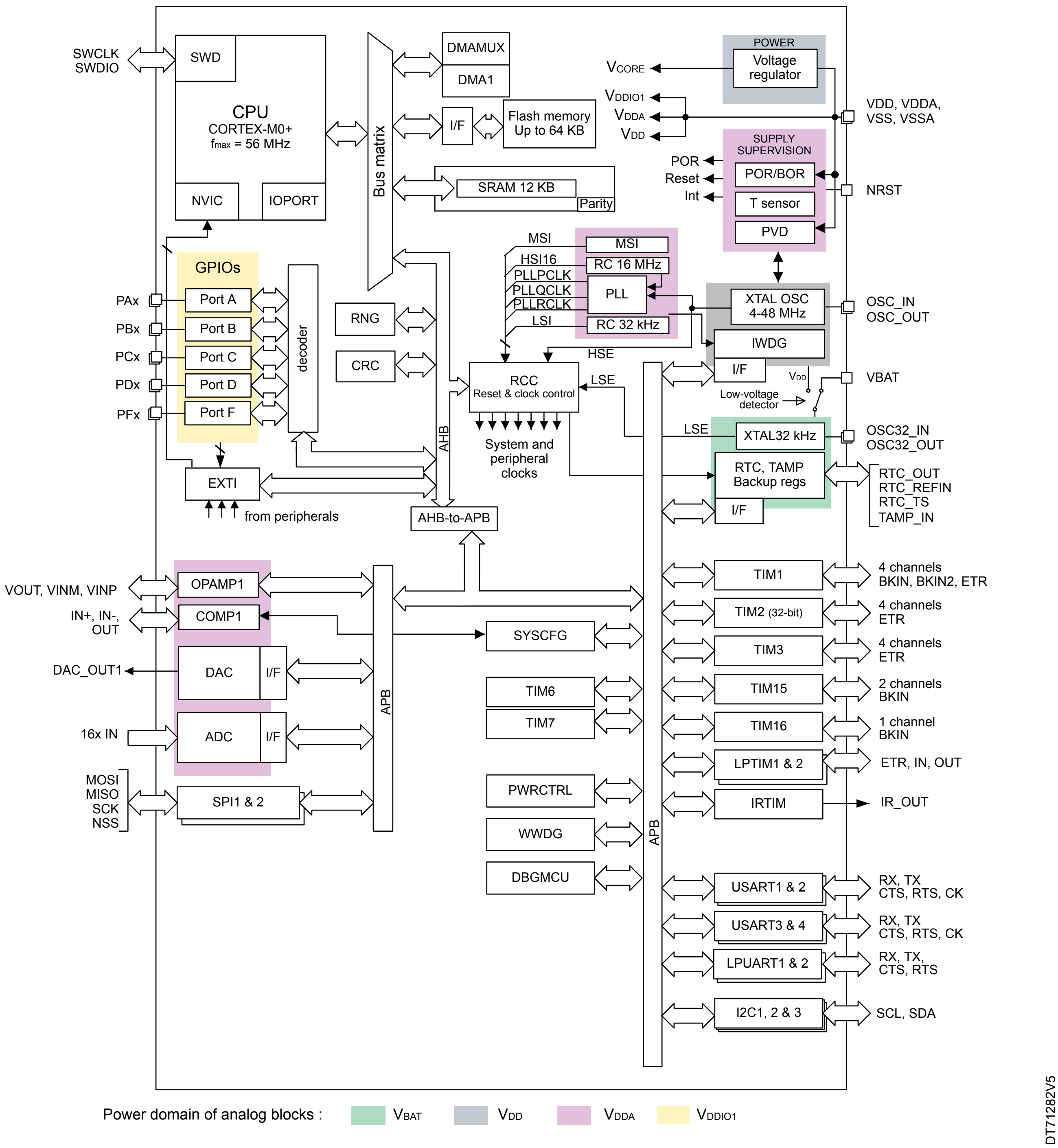
Refer to the table below for the list of peripherals available on each part number.

Table 1. **Device features and peripheral counts**

Peripherals		STM32U031R6	STM32U031R8	STM32U031C6	STM32U031C8	STM32U031K4	STM32U031K6	STM32U031K8	STM32U031G6	STM32U031G8	STM32U031F4	STM32U031F6	STM32U031F8
Flash memory (Kbytes)		32	64	32	64	16	32	64	32	64	16	32	64
SRAM (Kbytes)		12											
Timers	Advanced control	1 (16 bits)											
	General purpose	3 (16 bits) 1 (32 bits)											
	Basic	2 (16 bits)											
	Low	3 (16 bits)											
	SysTick	1											
	Watchdog timers (independent, window)	2											
Communication interfaces	SPI	2											
	I2C	3											
	USART	4											
	LPUART	2											
RTC		Yes											
Tamper pins		5		4		3			1		1		
TRNG		Yes											

Peripherals	STM32U031R6	STM32U031R8	STM32U031C6	STM32U031C8	STM32U031K4	STM32U031K6	STM32U031K8	STM32U031G6	STM32U031G8	STM32U031F4	STM32U031F6	STM32U031F8
GPIOs	53		39		27			24		17		
Wakeup pins	4		4		4			4		4		
Capacitive sensing Number of channels	18		12		7			6		3		
12-bit ADC	1											
Number of channels	16											
12-bit DAC	1											
Internal voltage reference buffer	None											
Analog comparator	1											
Operational amplifier	1											
Max. CPU frequency (MHz)	56											
Operating voltage (V_{DD})	1.71 to 3.6 V											
Operating temperature	Ambient operating temperature:-40 to 85 °C/-40 to 125 °C Junction temperature:-40 to 105 °C/-40 to 130 °C											
Packages	UFBGA64, LQFP64		UFQFPN48, LQFP48		UFQFPN32			WLCSP27		TSSOP20		

Figure 1. Block diagram



3 Functional overview

3.1 Arm® Cortex®-M0+ core with MPU

The Arm Cortex -M0+ is an entry-level 32-bit Arm Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- A simple architecture, easy to learn and program
- ultra-low power, energy-efficient operation
- Excellent code density
- Deterministic, high-performance interrupt handling
- Upward compatibility with Cortex-M processor family
- Platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area- and power-optimized 32-bit core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to embedded Arm core, the STM32U031x4/6/8 devices are compatible with Arm tools and software.

The Cortex-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC) described in Section 3.13.1: Nested vectored interrupt controller (NVIC).

3.2 Adaptive real-time memory accelerator (ART Accelerator)

The ART Accelerator is a memory accelerator optimized for STM32 industry-standard Arm® Cortex®-M0+ processors. It balances the inherent performance advantage of the Arm Cortex-M0+ over flash memory technologies, which normally requires the processor to wait for the flash memory at higher frequencies.

To release the processor near 67 DMIPS performance at 56 MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit flash memory. Based on benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from flash memory at a CPU frequency up to 56 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to corrupt accidentally the memory or resources used by any other active task.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Memories

3.4.1 Embedded flash memory

STM32U031x4/6/8 devices feature up to 64 Kbytes of embedded flash memory available for storing code and data.

Flexible protections can be configured thanks to option bytes:

- Robust readout protection (RDP) with password-based regression (128-bit PSWD). Three protections level states are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M0+ serial wire), boot in RAM and bootloader selection are disabled. This selection is irreversible.

  Refer to Table 2 for the memory area access versus the RDP protection level.
- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.

Table 2. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
User memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option memory	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup memory	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. *Erased upon RDP change from Level 1 to Level 0.*

The whole nonvolatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- Readout of the ECC fail address from the ECC register

Securable area

A part of the flash memory can be hidden from the application once the code it contains is executed. As soon as the security is enabled on the securable area through the FLASH_HDPCR and FLASH_SECR registers, the securable memory cannot be accessed until the system resets. The securable area generally contains the secure boot code to execute only once at boot. This helps to isolate secret code from untrusted application code.

3.4.2 Embedded SRAM

STM32U031x4/6/8 devices have 12-Kbyte SRAM with hardware parity check. Hardware parity check allows memory data errors to be detected, which contributes to increasing functional safety of applications.

The embedded SRAM is split between two regions, as follows:

- SRAM1: 8 Kbytes with hardware parity check, mapped at address 0x2000 0000
- SRAM2: 4 Kbytes with hardware parity check, located at address 0x1000 0000
  SRAM2 is also mapped at address 0x2000 8000, offering a contiguous address space with SRAM1 (4 Kbytes aliased by bit band).
  The content of SRAM2 is retained in Standby mode.
  It is write-protected with a 1-Kbyte granularity.

The memory can be read/write-accessed at CPU clock speed, with 0 wait states.

3.5 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- Boot from user flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot pin is shared with a standard GPIO and can be enabled through the boot selector option bit. The boot loader is located in system memory. It manages the flash memory reprogramming through one of the following interfaces:

- USART on pins PA9/PA10, PC10/PC11, or PA2/PA3
- I2C-bus on pins PB6/PB7 or PB10/PB11
- SPI on pins PA4/PA5/PA6/PA7 or PB12/PB13/PB14/PB15

3.6 Power supply management

3.6.1 Power supply schemes

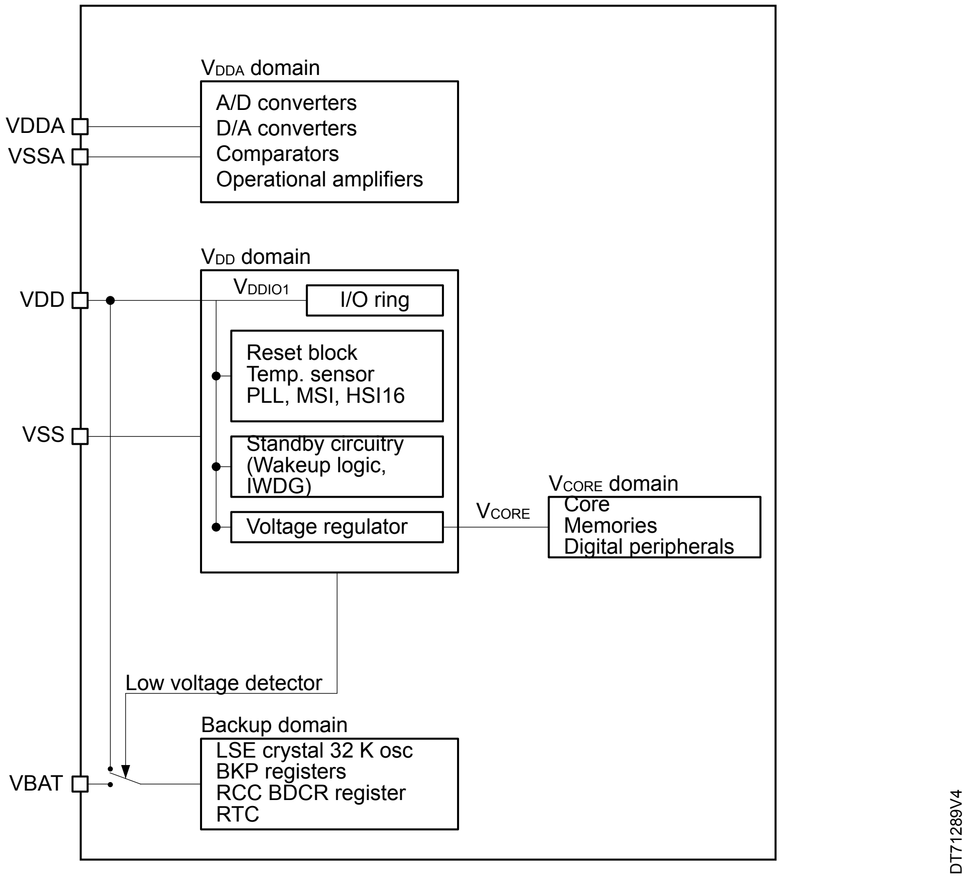
The STM32U031x4/6/8 devices require a 1.71 to 3.6 V operating supply voltage (V_{DD}).

Several different power supplies are provided to specific peripherals:

- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- V_{DDA} = 1.62 V (ADC/COMP)/1.80 V (DAC/OPAMP) to 3.6 V: external analog power supply for ADC, OPAMP, DAC, and comparator. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present. When VBAT pin is not available on the package, VBAT pad is internally bonded to VDD/VDDA pin.
- V_{CORE}
  An embedded linear voltage regulator is used to supply the V_{CORE} internal digital power. V_{CORE} is the power supply for digital peripherals, SRAM and flash memory. The flash memory is also supplied with V_{DD}.

Note: When the functions supplied by V_{DDA} are not used, this supply should preferably be shorted to V_{DD}.
If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant.
V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1}, with V_{DDIO1} = V_{DD}.

Figure 2. Power supply overview



3.6.2 Power supply supervisor

The device has an integrated power-on/power-down (POR/PDR) reset active in all power modes except Shutdown and ensuring proper operation upon power-on and power-down. It maintains the device in reset when the supply voltage is below $V_{POR/PDR}$ threshold, without the need for an external reset circuit. Brownout reset (BOR) function allows extra flexibility. It can be enabled and configured through option bytes, by selecting one of four thresholds for rising V_{DD} and other four for falling V_{DD}.

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to V_{PVD} threshold. It allows generating an interrupt when V_{DD} level crosses the V_{PVD} threshold, selectively while falling, while rising, or while falling and rising. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.6.3 Voltage regulator

Two embedded linear voltage regulators, main regulator (MR), and low-power regulator (LPR), supply most of digital circuitry in the device:

- The MR is used in Run, Sleep and Stop 0 modes.
- The LPR is used in Low-power run, Low-power sleep, Stop 1, and Stop 2 modes. It is also used to supply the 4-Kbyte SRAM2 in Standby mode, in order to ensure SRAM2 retention.

Both regulators are powered down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down, thus inducing zero consumption.

3.6.4 V_{BAT} operation

The V_{BAT} power domain, consuming very little energy, includes RTC, and LSE oscillator and backup registers.

In V_{BAT} mode, the RTC domain is supplied from VBAT pin. The power source can be, for example, an external battery or an external supercapacitor. Two anti-tamper detection pins are available.

The RTC domain can also be supplied from VDD/VDDA pin.

By means of a built-in switch, an internal voltage supervisor allows automatic switching of RTC domain powering between V_{DD} and voltage from V_{BAT} pin to ensure that the supply voltage of the RTC domain (V_{BAT}) remains within valid operating conditions. If both voltages are valid, the RTC domain is supplied from VDD/VDDA pin.

An internal circuit for charging the battery on VBAT pin can be activated if the V_{DD} voltage is within a valid range.

Note: External interrupts and RTC alarm/events cannot cause the microcontroller to exit the VBAT mode, as in that mode the V_{DD} is not within a valid range.

3.7 Low-power modes

By default, the microcontroller is in Run mode after system or power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run mode**
  This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator operating current. The code can be executed from SRAM or from flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep mode**
  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When the wake-up is triggered by an event or an interrupt, the system reverts to the Low-power run mode.
- **Stop 0, Stop 1, and Stop 2 modes**
  The Stop modes achieve a lowest power consumption while retaining the content of SRAM and registers. All the clocks in the V_{CORE} domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE and LSI clocks are still running.
  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).
  Some peripherals with the wake-up capability can enable the HSI16 RC during Stop mode, to detect their wake-up condition.
  Three Stop modes are available, Stop 0, Stop 1 and Stop2:
  – In Stop2 mode, most of the V_{CORE} domain is put in lower-leakage mode.
  – Stop 1 offers the largest number of active peripherals and wake-up sources, a smaller wake-up time, but with a higher consumption than Stop 2 mode.
  – In Stop 0 mode, the main regulator remains on, allowing a very fast wake-up time, but with a much higher consumption.

  When exiting from Stop 0, Stop 1 or Stop 2 mode, the system clock can be either the MSI clock (up to 48 MHz) or HSI16, depending on software configuration.
- **Standby mode**
  The Standby mode is used to achieve one of the lowest power consumption, with POR/PDR always active in this mode. The main regulator is switched off to power down V_{CORE} domain. The low-power regulator is either switched off or kept active. In the latter case, it only supplies SRAM to ensure data retention. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are also powered down. The RTC can remain active (Standby mode with RTC, Standby mode without RTC).
  For each I/O, the software can determine whether a pull-up, a pull-down or no resistor must be applied to that I/O during Standby mode.
  Upon entering Standby mode, register contents are lost except for registers in the RTC domain and standby circuitry. The SRAM contents can be retained through register setting.
  The device exits Standby mode upon external reset event (NRST pin), IWDG reset event, wake-up event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wake-up, timestamp, tamper), or when a failure is detected on LSE (CSS on LSE).
- **Shutdown mode**
  The Shutdown mode enables to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.
  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).
  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.
  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.
  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wake-up, timestamp, tamper).
  The system clock after wake-up is MSI at 4 MHz.

Table 3. **Functionalities depending on the mode**

Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (up to 64 Kbytes)	O(1)	O(1)	O(1)	O(1)	-	-	-	-	-	-	-	-	-
SRAM1 (8 Kbytes)	Y	Y(2)	Y	Y(2)	Y	-	Y	-	-	-	-	-	-
SRAM2 (4 Kbytes)	Y	Y(2)	Y	Y(2)	Y	-	Y	-	O(3)	-	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor (PVMx; x = 1, 2, 3)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
High-speed Internal (HSI16)	O	O	O	O	(4)	-	(4)	-	-	-	-	-	-
High-speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low-speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi-Speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto-wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC tamper pins	2	2	2	2	2	O	2	O	2	O	2	O	2
USARTx (x = 1, 2, 3, 4)	O	O	O	O	O(5)	O(5)	-	-	-	-	-	-	-
LPUARTx (x = 1 to x = 2)	O	O	O	O	O(5)	O(5)	O(5)	O(5)	-	-	-	-	-
I2Cx (x = 2)	O	O	O	O	O(6)	O(6)	-	-	-	-	-	-	-
I2Cx (x = 1, 3)	O	O	O	O	O(6)	O(6)	O(6)	O(6)	-	-	-	-	-
SPIx (x = 1 to 2)	O	O	O	O	-	-	-	-	-	-	-	-	-
ADC1	O	O	O	O	-	-	-	-	-	-	-	-	-
DAC1	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMP1	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x = 1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
LPTIMx (x = 1 to 2)	O	O	O	O	O	O	O	O	-	-	-	-	-

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
True random number generator (RNG)	O(7)	O(7)	-	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(8)	5 pins(9)	(10)	5 pins(9)	-

1. *The flash memory can be configured in power-down mode. By default, it is not in power-down mode.*
2. *The SRAM clock can be gated on or off.*
3. *SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.*
4. *Some peripherals with wake-up from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.*
5. *UART and LPUART reception is functional in Stop mode, and generates a wake-up interrupt on Start, address match or received frame event.*
6. *I2C address detection is functional in Stop mode, and generates a wake-up interrupt in case of address match.*
7. *Voltage scaling Range 1 only.*
8. *I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.*
9. *The I/Os with wake-up from Standby/Shutdown capability are PA0, PA1, PA2, PB15, PC5, and PC13.*
10. *I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.*

3.8 Peripheral interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

Table 4. **Interconnect of peripherals**

Interconnect source	Interconnect destination	Interconnect action	Run Low-power run	Sleep Low-power sleep	Stop
TIMx	TIMx	Timer synchronization or chaining	Y	Y	-
	ADCx DACx	Conversion triggers	Y	Y	-
	DMA	Memory-to-memory transfer trigger	Y	Y	-
	COMPx	Comparator output blanking	Y	Y	-
COMPx	TIM1, 2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	-
	LPTIMx	Low-power timer triggered by analog signals comparison	Y	Y	Y
ADCx	TIM1	Timer triggered by analog watchdog	Y	Y	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	-
	LPTIMx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y
All clock sources (internal and external)	TIM16	Clock source used as input channel for RC measurement and trimming	Y	Y	-
CSS RAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1, 15, 16	Timer break	Y	Y	-
CPU (HardFault)	TIM1 15, 16	Timer break	Y	-	-
GPIOs	TIMx	External trigger	Y	Y	-
	LPTIMx	External trigger	Y	Y	Y
	ADCx DACx	Conversion external trigger	Y	Y	-

3.9 Reset and clock controller (RCC)

3.9.1 Reset mode

During and upon exiting reset, the schmitt triggers of I/Os are disabled so as to reduce power consumption. In addition, when the reset source is internal, the built-in pull-up resistor on NRST pin is deactivated.

3.9.2 Clocks and startup

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.

- **Safe clock** switching: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**: two different sources can deliver SYSCLK system clock:
  - 4-48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). It can supply clock to system PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software. It can supply clock to system PLL.
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies form 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach an accuracy better than ± 0.25%. The MSI can supply a PLL.
  - System PLL, which can be fed by HSE, HSI16 or MSI. It provides a system clock up to 56 MHz.
- **Auxiliary clock source**: three ultra-low-power clock sources for the real-time clock (RTC):
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ± 5% accuracy, also used to clock an independent watchdog.
- **Peripheral clock sources**: several peripherals (RNG, USARTs, I2Cs, LPTIMs, ADC) have their own clock independent of the system clock.
- **Clock security system (CSS)**: in the event of HSE clock failure, the system clock is automatically switched to HSI16 and, if enabled, a software interrupt is generated. LSE clock failure can also be detected and generate an interrupt. The CSS feature can be enabled by software.
- **Clock output**:
  - **MCO (microcontroller clock output)** provides one of the internal clocks for external use by the application
  - **LSCO (low speed clock output)** provides LSI or LSE in all low-power modes (except in VBAT operation).

Several prescalers enable the application to configure AHB and APB domain clock frequencies, 56 MHz at maximum.

3.10 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function (AF). Most of the GPIO pins are shared with special digital or analog functions.

Through a specific sequence, this special function configuration of I/Os can be locked, such as to avoid spurious writing to I/O control registers.

3.11 Direct memory access controller (DMA)

The direct memory access (DMA) controller is a bus master and system peripheral with single-AHB architecture.

With seven channels, it performs data transfers between memory-mapped peripherals and/or memories, to offload the CPU.

Each channel is dedicated to managing memory access requests from one or more peripherals. The unit includes an arbiter for handling the priority between DMA requests.

Main features of the DMA controller:

- Single-AHB master
- Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-to-peripheral data transfers
- Access, as source and destination, to on-chip memory-mapped devices such as flash memory, SRAM, and AHB and APB peripherals
- All DMA channels independently configurable:
  - Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
  - Priority between the requests is programmable by software (four levels per channel: very high, high, medium, low) and by hardware in case of equality (such as request to channel 1 has priority over request to channel 2).
  - Transfer size of source and destination are independent (byte, half-word, word), emulating packing and unpacking. Source and destination addresses must be aligned on the data size.
  - Support of transfers from/to peripherals to/from memory with circular buffer management
  - Programmable number of data to be transferred: 0 to 2^{16} - 1
- Generation of an interrupt request per channel. Each interrupt request originates from any of the three DMA events: transfer complete, half transfer, or transfer error.

3.12 DMA request multiplexer (DMAMUX)

The DMAMUX request multiplexer enables routing a DMA request line between the peripherals and the DMA controller. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. DMAMUX may also be used as a DMA request generator from programmable events on its input trigger signals.

3.13 Interrupts and events

The device flexibly manages events causing interrupts of linear program execution, called exceptions. The Cortex®-M0+ processor core, a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI) are the assets contributing to handling the exceptions. Exceptions include core-internal events such as, for example, a division by zero and, core-external events such as logical level changes on physical lines. Exceptions result in interrupting the program flow, executing an interrupt service routine (ISR) then resuming the original program flow.

The processor context (contents of program pointer and status registers) is stacked upon program interrupt and unstacked upon program resume, by hardware. This avoids context stacking and unstacking in the interrupt service routines (ISRs) by software, thus saving time, code and power. The ability to abandon and restart load-multiple and store-multiple operations significantly increases the device’s responsiveness in processing exceptions.

3.13.1 Nested vectored interrupt controller (NVIC)

The configurable nested vectored interrupt controller is tightly coupled with the core. It handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupts, and Cortex®-M0+ exceptions. It provides flexible priority management.

The tight coupling of the processor core with NVIC significantly reduces the latency between interrupt events and start of corresponding interrupt service routines (ISRs). The ISR vectors are listed in a vector table, stored in the NVIC at a base address. The vector address of an ISR to execute is hardware-built from the vector table base address and the ISR order number used as offset.

If a higher-priority interrupt event happens while a lower-priority interrupt event occurring just before is waiting for being served, the later-arriving higher-priority interrupt event is served first. Another optimization is called tail-chaining. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context unstacking and stacking is skipped. This reduces latency and contributes to power efficiency.

Features of the NVIC:

- Low-latency interrupt processing
- Four priority levels
- Handling of a non-maskable interrupt (NMI)
- Handling of 32 maskable interrupt lines
- Handling of 10 Cortex-M0+ exceptions
- Later-arriving higher-priority interrupt processed first
- Tail-chaining
- Interrupt vector retrieval by hardware

3.13.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller adds flexibility in handling physical line events and allows identifying wake-up events at processor wake-up from Stop mode.

The EXTI controller has a number of channels, of which some with rising, falling or rising, and falling edge detector capability. Any GPIO and a few peripheral signals can be connected to these channels.

The channels can be independently masked.

The EXTI controller can capture pulses shorter than the internal clock period.

A register in the EXTI controller latches every event even in Stop mode, which enables the software to identify the origin of the processor wake-up from Stop mode or, to identify the GPIO and the edge event having caused an interrupt.

3.14 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

3.15 Analog-to-digital converter (ADC)

A native 12-bit analog-to-digital converter is embedded into STM32U031x4/6/8 devices. It can be extended to 16-bit resolution through hardware oversampling. The ADC has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference, V_{BAT} monitoring). It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of ~2 Msps even with a low CPU speed. An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate in the whole V_{DD} supply range.

The ADC features a hardware oversampler up to 256 samples, improving the resolution to 16 bits (refer to AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions with timers.

3.15.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to an ADC input to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor may vary from part to part due to process variation, the uncalibrated internal temperature sensor is suitable only for relative temperature measurements.

To improve the accuracy of the temperature sensor, each part is individually factory-calibrated by ST. The resulting calibration data are stored in the part's engineering bytes, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA} = 3.0 V (± 10 mV)	0x1FFF 6E68 - 0x1FFF 6E69
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), V_{DDA} = 3.0 V (± 10 mV)	0x1FFF 6E8A - 0x1FFF 6E8B

3.15.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to an ADC input. The V_{REFINT} voltage is individually precisely measured for each part by ST during production test and stored in the part's engineering bytes. It is accessible in read-only mode.

Table 6. Internal voltage reference calibration values

Calibration value name	Description	Memory address
V_{REFINT}	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA} = 3.0 V (± 10 mV)	0x1FFF 6EA4 - 0x1FFF 6EA5

3.15.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using an internal ADC input. As the V_{BAT} voltage may be higher than V_{DDA} and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by three. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.16 Digital-to-analog converter (DAC)

The single-channel 12-bit buffered DAC converts a digital value into an analog voltage available on the channel output. The architecture of either channel is based on integrated resistor string and an inverting amplifier.

Features of the DAC:

- One DAC output channel
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability
- Triggering with timer events, synchronized with DMA
- Triggering with external events
- Sample-and-hold low-power mode, with internal or external capacitor

3.17 Comparators (COMP)

STM32U031x4/6/8 embed an embedded rail-to-rail analog comparator with programmable reference voltage (internal or external), hysteresis, speed (low for low-power), and output polarity.

The reference voltage can be one of the following:

- External, from an I/O
- Internal, from DAC
- Internal reference voltage (V_{REFINT}) or its submultiple (1/4, 1/2, 3/4)

The comparators can wake up the device from Stop mode, generate interrupts, breaks or triggers for the timers and can be also combined into a window comparator.

3.18 Operational amplifier (OPAMP)

The STM32U031x4/6/8 devices embed one operational amplifier with external and internal follower routing and PGA capability.

Features of the operational amplifier:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.19 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (such as glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library that is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Charge transfer acquisition principle
- Up to 18 capacitive sensing channels
- Up to three capacitive sensing channels can be acquired in parallel offering a very good response time
- Five selectable thresholds (V_{IH}, V_{REF}, 3/4 V_{REF}, 1/2 V_{REF}, 1/4 V_{REF}) using the digital threshold or the ultra-low-power comparator
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to three capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with the STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.20 True random-number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

3.21 Timers and watchdogs

The device includes an advanced-control timer, six general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer. Table 7 compares features of the advanced-control, general-purpose and basic timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Maximum operating frequency	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced-control	TIM1	16-bit	Up, down, up/down	56 MHz	Integer from 1 to 2^{16}	Yes	4	3
General -purpose	TIM2	32-bit	Up, down, up/down	56 MHz	Integer from 1 to 2^{16}	Yes	4	-
	TIM3	16-bit	Up, down, up/down	56 MHz	Integer from 1 to 2^{16}	Yes	4	-
	TIM15	16-bit	Up	56 MHz	Integer from 1 to 2^{16}	Yes	2	1
	TIM16	16-bit	Up	56 MHz	Integer from 1 to 2^{16}	Yes	1	1
Basic	TIM6 and TIM7	16-bit	Up	56 MHz	Integer from 1 to 2^{16}	Yes	-	-
Lower-power	LPTIM1 and LPTIM2	16-bit	Up	56 MHz	2^n where n = 0 to 7	No	N/A	-

3.21.1 Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM unit multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM output (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled, so as to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in Section 3.21.2: General-purpose timers (TIM2, 3, 15, 16)) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.21.2 General-purpose timers (TIM2, 3, 15, 16)

There are four synchronizable general-purpose timers embedded in the device (refer to Table 7 for comparison). Each general-purpose timer can be used to generate PWM outputs or act as a simple timebase.

- TIM2, TIM3
  These are full-featured general-purpose timers:
  - TIM2 with 32-bit auto-reload up/downcounter and 16-bit prescaler
  - TIM3 with 16-bit auto-reload up/downcounter and 16-bit prescaler

  They have four independent channels for input capture/output compare, PWM, or onepulse mode output. They can operate together or in combination with other general-purpose timers via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request and support quadrature encoders. Their counters can be frozen in debug mode.
- TIM15, TIM16
  These are general-purpose timers featuring:
  - 16-bit auto-reload upcounter and 16-bit prescaler
  - 2 channels and 1 complementary channel for TIM15
  - 1 channel and 1 complementary channel for TIM16

  All channels can be used for input capture/output compare, PWM or one-pulse mode output. The timers can operate together via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request. Their counters can be frozen in debug mode.

3.21.3 Basic timers (TIM6 and TIM7)

These timers are mainly used for triggering DAC conversions. They can also be used as generic 16-bit timebases.

3.21.4 Low-power timers (LPTIM1 and LPTIM2)

These timers have an independent clock. When fed with LSE, LSI or external clock, they keep running in Stop mode and they can wake up the system from it.

Features of LPTIM1 and LPTIM2:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output (pulse, PWM)
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Selectable clock source:
  - Internal: LSE, LSI, HSI16 or APB clocks
  - External: over LPTIM input (working even with no internal clock source running, used by pulse counter application)
- Programmable digital glitch filter
- Encoder mode

3.21.5 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 32 kHz internal RC (LSI).

Independent of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. Its counter can be frozen in debug mode.

3.21.6 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked by the system clock. It has an early-warning interrupt capability. Its counter can be frozen in debug mode.

3.21.7 SysTick timer

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter.

Features of SysTick timer:

- 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.22 Real-time clock (RTC), tamper (TAMP) and backup registers

The device embeds an RTC and nine 32-bit backup registers, located in the RTC domain of the silicon die.

The ways of powering the RTC domain are described in Section 3.6.1: Power supply schemes.

The RTC is an independent BCD timer/counter.

Features of the RTC:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Programmable alarm
- On-the-fly correction from 1 to 32767 RTC clock pulses, usable for synchronization with a master clock
- Reference clock detection - a more precise second-source clock (50 or 60 Hz) can be used to improve the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Five anti-tamper detection pins with programmable filter
- Timestamp feature to save a calendar snapshot, triggered by an event on the timestamp pin or a tamper event, or by switching to VBAT mode
- 17-bit auto-reload wake-up timer (WUT) for periodic events, with programmable resolution and period
- Multiple clock sources and references:
  - A 32.768 kHz external crystal (LSE)
  - An external resonator or oscillator (LSE)
  - The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
  - The high-speed external clock (HSE) divided by 32

When clocked by LSE, the RTC operates in VBAT mode and in all low-power modes. When clocked by LSI, the RTC does not operate in VBAT mode, but it does in low-power modes except for the Shutdown mode.

All RTC events (alarm, wake-up timer, timestamp or tamper) can generate an interrupt and wake the device up from the low-power modes.

The backup registers allow keeping 20 bytes of user application data in the event of VDD failure, if a valid backup supply voltage is provided on VBAT pin. They are not affected by the system reset, power reset, and upon the device wake-up from Standby or Shutdown modes.

3.23 Inter-integrated circuit interface (I2C)

The device embeds three I2C peripherals. Refer to Table 8 for the features.

The I^{2}C-bus interface handles communication between the microcontroller and the serial I^{2}C-bus. It controls all I^{2}C-bus-specific sequencing, protocol, arbitration and timing.

Features of the I2C peripheral:

- I^{2}C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and extra output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Clock stretching

- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent of the PCLK reprogramming
- Wake-up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 8. I^2C implementation

I^2C features	I2C1	I2C2	I2C3
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast mode Plus (up to 1 Mbit/s) with extra output drive I/Os	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	-	-	-
Independent clock	X	-	X
Wakeup from Stop mode on address match	X	-	X

3.24 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The devices embed universal synchronous/asynchronous receivers/transmitters that communicate at speeds of up to 8 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, synchronous SPI master/slave communication and single-wire half-duplex communication mode. Some can also support smartcard communication (ISO 7816), IrDA SIR ENDEC, LIN master/slave capability and auto baud rate feature, and have a clock domain independent of the CPU clock, which allows them to wake up the MCU from Stop mode. The wake-up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 9. USART implementation

X: supported

USART modes/ features	USART1 USART2	USART3 USART4
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous SPI mode (master/slave)	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wake-up from Stop mode	X	-

USART modes/ features	USART1 USART2	USART3 USART4
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver enable	X	X

3.25 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed two LPUARTs. The peripherals support asynchronous serial communication with minimum power consumption, as well as half-duplex single wire communication and modem operations (CTS/RTS). They allow multiprocessor communication.

The LPUARTs have a clock domain independent of the CPU clock, and can wake up the system from Stop mode using baud rates up to 220 Kbaud. The Stop mode wake-up events are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUARTs can wait for an incoming frame while having an extremely low energy consumption. To reach higher baud rates, a higher speed clock can be used.

The LPUART interface can be served by the DMA controller.

3.26 Serial peripheral interface (SPI)

The devices contain two SPIs running at up to 32 Mbits/s in master and slave modes. It supports half-duplex, full-duplex and simplex communications. A 3-bit prescaler gives eight master mode frequencies. The frame size is configurable from 4 bits to 16 bits. The SPI peripherals support NSS pulse mode, TI mode and hardware CRC calculation.

The SPI peripherals can be served by the DMA controller.

Table 10. SPI implementation

X: supported

SPI modes/ features	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I2S mode	-	-
TI mode	X	X

3.27 Debug support

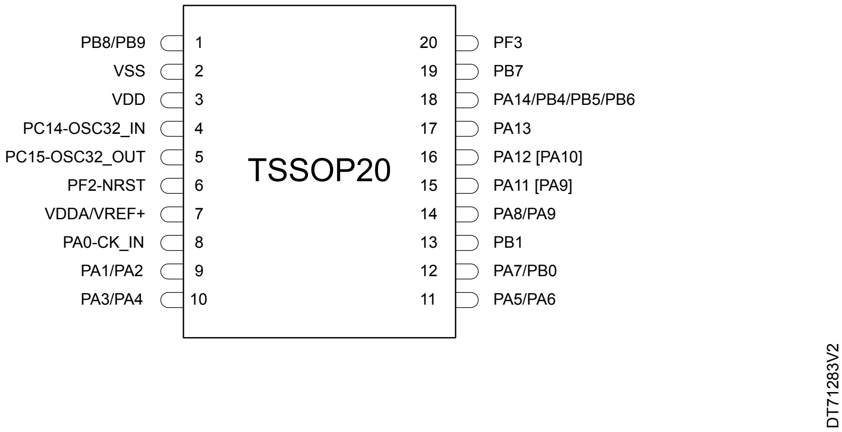
3.27.1 Serial wire debug port (SW-DP)

An Arm® SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts/ballouts, pin description, and alternate functions

4.1 Pinout/ballout schematics

Figure 3. TSSOP20 pinout



1. *The above figure shows the package top view.*

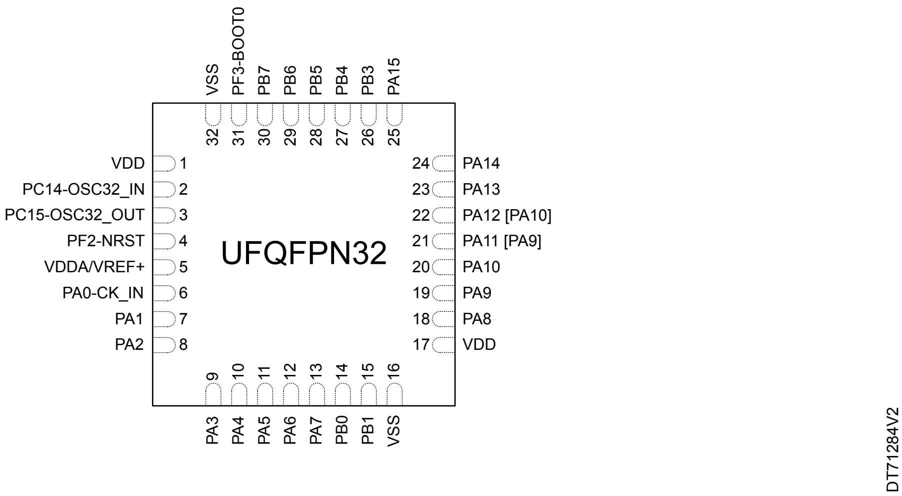
Figure 4. WLCSP27 ballout

	1	2	3	4	5	6	7	8	9
A	NC	PB6	NC	PB7	NC	PF3-BOOT0	NC	VSS	NC
B	PA14	NC	PB5	NC	PA12 [PA10]	NC	VDD	NC	PC14-OSC32_IN
C	NC	PA13	NC	PA11 [PA9]	NC	PA0-CK_IN	NC	PC15-OSC32_OUT	NC
D	PA10	NC	PA9	NC	PA6	NC	PA1	NC	PF2-NRST
E	NC	PA8	NC	PA7	NC	PA5	NC	PA2	NC
F	PB1	NC	PB0	NC	PA4	NC	PA3	NC	VDDA/ VREF+

DT71291V3

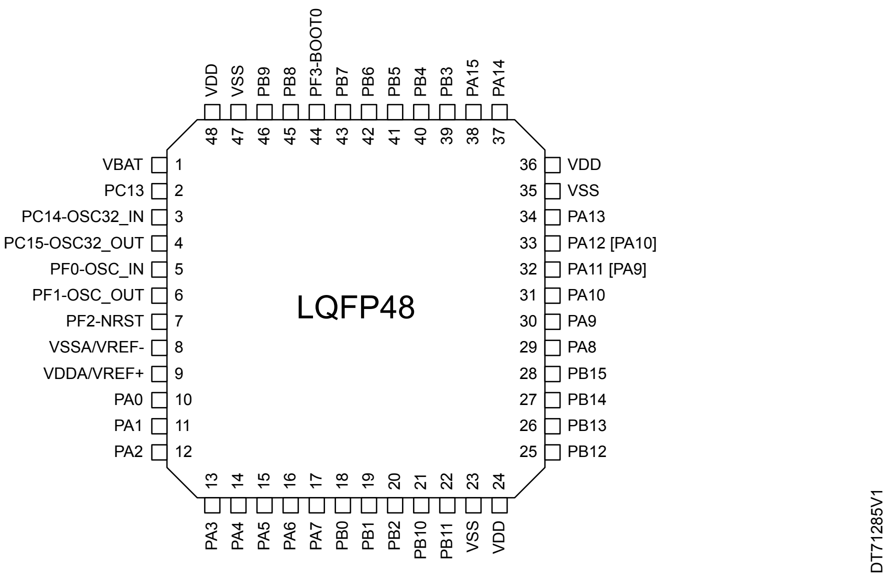
1. *The above figure shows the package top view.*
2. *The nonconnected pads are grayed.*

Figure 5. UFQFPN32 pinout



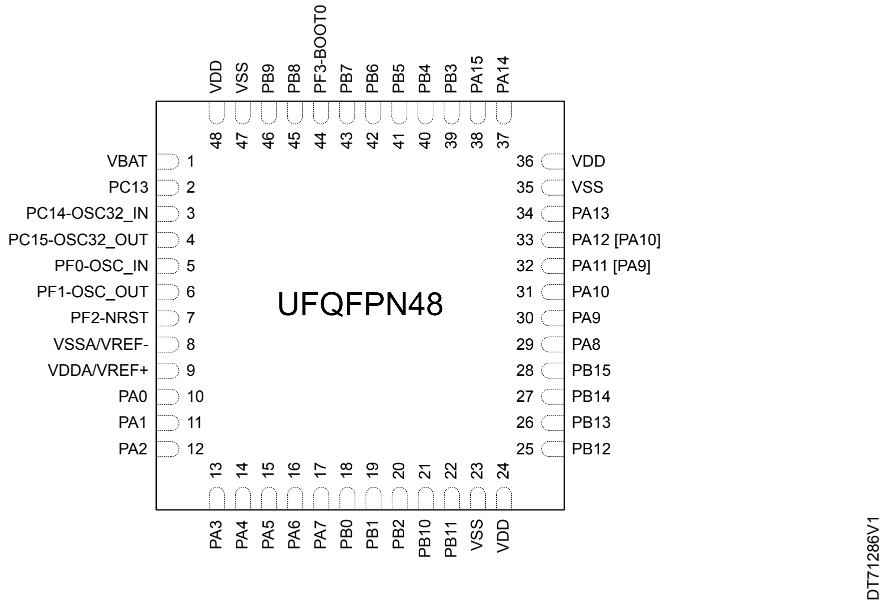
1. *The above figure shows the package top view.*

Figure 6. LQFP48 pinout



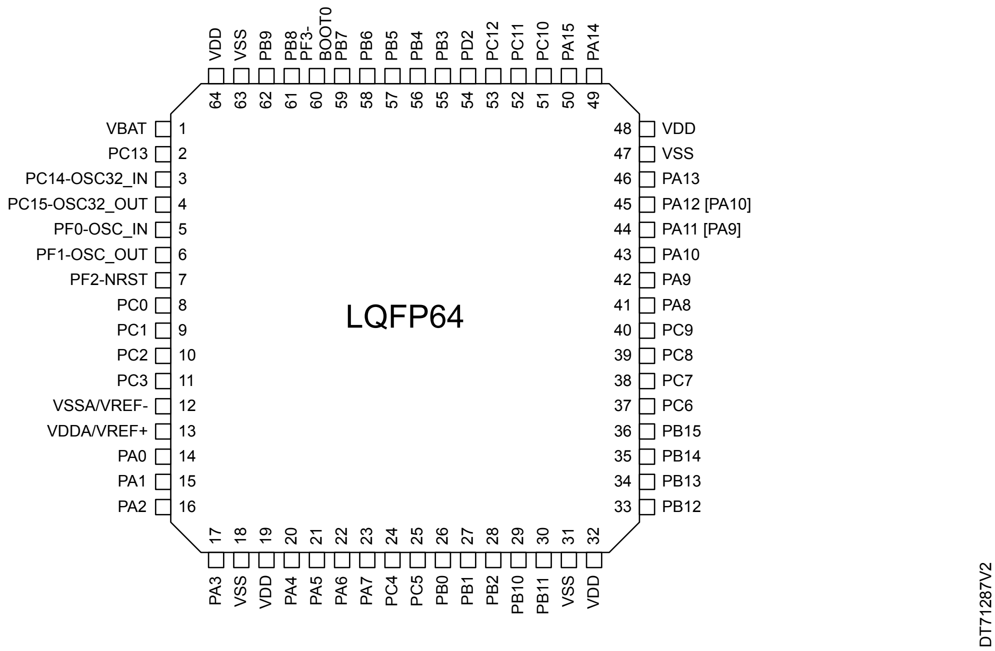
1. *The above figure shows the package top view.*

Figure 7. UFQFPN48 pinout



1. *The above figure shows the package top view.*

Figure 8. LQFP64 pinout



1. *The above figure shows the package top view.*

Figure 9. UFBGA64 ballout

	1	2	3	4	5	6	7	8
A	PC14-OSC32_IN	PC13	PB9	PB4	PB3	PA15	PA14	PA13
B	PC15-OSC32_OUT	VBAT	PB8	PF3-BOOT0	PD2	PC11	PC10	PA12 [PA10]
C	PF0-OSC_IN	VSS	PB7	PB5	PC12	PA10	PA9	PA11 [PA9]
D	PF1-OSC_OUT	VDD	PB6	VSS	VSS	VSS	PA8	PC9
E	PF2-NRST	PC1	PC0	VDD	VDD	VDD	PC7	PC8
F	VSSA/VREF-	PC2	PA2	PA5	PB0	PC6	PB15	PB14
G	PC3	PA0	PA3	PA6	PB1	PB2	PB10	PB13
H	VDDA/VREF+	PA1	PA4	PA7	PC4	PC5	PB11	PB12

DT71288V2

1. *The above figure shows the package top view.*

4.2 Pin description

Table 11. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I/O	Input /output pin
I/O structure		FT	5V-tolerant I/O
		TT	3.6V-tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Options for TT and FT I/Os	
		_a	I/O with analog switch function supplied by V_{DDA}
		_f	I2C Fm+ capable I/O
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. STM32U031x4/6/8 pin/ball definition

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP27	UFQFPN32	LQFP48	UFQFPN48	LQFP64	UFBGA64						
-	-	-	1	1	1	B2	VBAT	S	-	-	-	-
-	-	-	2	2	2	A2	PC13	I/O	FT	(1)(2)	LPTIM1_CH3, EVENTOUT	WKUP2, TAMP_IN1, RTC_TS/RTC_OUT1
4	B9	2	3	3	3	A1	PC14-OSC32_IN	I/O	FT	(1)(2)	EVENTOUT	OSC32_IN
5	C8	3	4	4	4	B1	PC15-OSC32_OUT	I/O	FT	(1)(2)	OSC32_EN, OSC_EN, EVENTOUT	OSC32_OUT, OSC32_EN
-	A8	-	-	-	-	C2	VSS	S	-	-	-	-
-	-	-	-	-	-	E4	VDD	S	-	-	-	-
-	-	-	5	5	5	C1	PF0-OSC_IN	I/O	FT	-	EVENTOUT	OSC_IN

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP27	UFQFPN32	LQFP48	UFQFPN48	LQFP64	UFBGA64						
-	-	-	6	6	6	D1	PF1-OSC_OUT	I/O	FT	-	OSC_EN, EVENTOUT	OSC_OUT
6	D9	4	7	7	7	E1	PF2-NRST	I/O	RST	-	MCO	NRST
-	-	-	-	-	8	E3	PC0	I/O	FT_fa	-	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LPUART2_TX, LPTIM2_IN1, EVENTOUT	ADC1_IN1
-	-	-	-	-	9	E2	PC1	I/O	FT_fa	-	LPTIM1_CH1, I2C3_SDA, LPUART1_TX, LPUART2_RX, EVENTOUT	ADC1_IN2
-	-	-	-	-	10	F2	PC2	I/O	FT_a	-	MCO2, LPTIM1_IN2, SPI2_MISO, EVENTOUT	ADC1_IN3
-	-	-	-	-	11	G1	PC3	I/O	FT_a	-	LPTIM1_ETR, SPI2_MOSI, USART4_CK, LPTIM2_ETR, EVENTOUT	ADC1_IN4
-	-	-	8	8	12	F1	VSSA/VREF-	S	-	-	-	-
7	F9	5	9	9	13	H1	VDDA/VREF+	S	-	-	-	-
-	-	-	10	10	14	G2	PA0	I/O	FT_a	-	TIM2_CH1, USART2_CTS, USART4_TX, COMP1_OUT, TIM2_ETR, EVENTOUT	OPAMP1_VINP, COMP1_INM3, ADC1_IN5, WKUP1, TAMP_IN2
8	C6	6	-	-	-	-	PA0-CK_IN	I/O	FT_a	-	TIM2_CH1, USART2_CTS, USART4_TX, COMP1_OUT, TIM2_ETR, EVENTOUT	OPAMP1_VINP, COMP1_INM3, ADC1_IN5, WKUP1, TAMP_IN2
9	D7	7	11	11	15	H2	PA1	I/O	FT_a	-	TIM2_CH2, LPTIM1_CH2, SPI1_SCK, SPI2_SCK, USART2_RTS/USART2_DE, USART4_RX, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, COMP1_INP3, ADC1_IN6, WKUP3, TAMP_IN5
9	E8	8	12	12	16	F3	PA2	I/O	FT_a	-	TIM2_CH3, USART2_TX, LPUART1_TX, TIM15_CH1, EVENTOUT	ADC1_IN7, WKUP4/LSCO
10	F7	9	13	13	17	G3	PA3	I/O	TT_a	-	TIM2_CH4, USART2_RX, LPUART1_RX, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, ADC1_IN8
-	-	-	-	-	18	-	VSS	S	-	-	-	-
-	-	-	-	-	19	D2	VDD	S	-	-	-	-
10	F5	10	14	14	20	H3	PA4	I/O	TT_a	-	SPI1_NSS, USART2_CK, LPTIM2_CH1, EVENTOUT	COMP1_INM4, ADC1_IN9, DAC1_OUT1
11	E6	11	15	15	21	F4	PA5	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, USART3_TX, LPTIM2_ETR, EVENTOUT	COMP1_INM5, ADC1_IN10
11	D5	12	16	16	22	G4	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, I2C2_SDA, I2C3_SDA, SPI1_MISO, COMP1_OUT, USART3_CTS, LPUART1_CTS, TSC_G5_IO1, TIM16_CH1, EVENTOUT	ADC1_IN11
12	E4	13	17	17	23	H4	PA7	I/O	FT_fa	-	TIM1_CH1N, TIM3_CH2, I2C2_SCL, I2C3_SCL, SPI1_MOSI, USART3_RX, LPTIM2_CH2, EVENTOUT	ADC1_IN15
-	-	-	-	-	24	H5	PC4	I/O	FT_a	-	USART3_TX, EVENTOUT	COMP1_INM1, ADC1_IN16

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP27	UFQFPN32	LQFP48	UFQFPN48	LQFP64	UFBGA64						
-	-	-	-	-	25	H6	PC5	I/O	FT_a	-	USART3_RX, EVENTOUT	COMP1_INP1, ADC1_IN17, WKUP5, TAMP_IN4
12	F3	14	18	18	26	F5	PB0	I/O	FT_a	-	TIM1_CH2N, TIM3_CH3, SPI1_NSS, USART3_CK, LPUART2_CTS, TSC_G5_IO2, COMP1_OUT, EVENTOUT	ADC1_IN18
13	F1	15	19	19	27	G5	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, USART3_RTS/ USART3_DE, LPUART1_RTS/LPUART1_DE, TSC_SYNC, LPUART2_RTS/LPUART2_DE, LPTIM2_IN1, EVENTOUT	COMP1_INM2, ADC1_IN19
-	-	-	20	20	28	G6	PB2	I/O	FT_a	-	RTC_OUT2, LPTIM1_CH1, EVENTOUT	COMP1_INP2, RTC_OUT2
-	-	-	21	21	29	G7	PB10	I/O	FT_f	-	TIM2_CH3, I2C2_SCL, SPI2_SCK, USART3_TX, LPUART1_RX, TSC_G5_IO3, LPUART2_RX, COMP1_OUT, EVENTOUT	-
-	-	-	22	22	30	H7	PB11	I/O	FT_f	-	TIM2_CH4, I2C2_SDA, USART3_RX, LPUART1_TX, TSC_G5_IO4, LPUART2_TX, EVENTOUT	-
-	-	16	23	23	31	-	VSS	S	-	-	-	-
-	-	-	-	-	-	D6	VSS	S	-	-	-	-
-	B7	17	24	24	32	E6	VDD	S	-	-	-	-
-	-	-	25	25	33	H8	PB12	I/O	FT	-	TIM1_BKIN, SPI2_NSS, USART3_CK, LPUART1_RTS/LPUART1_DE, TSC_G1_IO1, TIM15_BKIN, EVENTOUT	-
-	-	-	26	26	34	G8	PB13	I/O	FT_f	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, TIM15_CH1N, EVENTOUT	-
-	-	-	27	27	35	F8	PB14	I/O	FT_f	-	TIM1_CH2N, I2C2_SDA, SPI2_MISO, USART3_RTS/USART3_DE, TSC_G1_IO3, TIM15_CH1, EVENTOUT	-
-	-	-	28	28	36	F7	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, TSC_G1_IO4, TIM15_CH2, EVENTOUT	WKUP7, TAMP_IN3
-	-	-	-	-	37	F6	PC6	I/O	FT_a	-	TIM3_CH1, LPUART2_TX, TSC_G4_IO1, EVENTOUT	COMP1_INP5
-	-	-	-	-	38	E7	PC7	I/O	FT	-	TIM3_CH2, LPUART2_RX, TSC_G4_IO2, LPTIM2_CH2, EVENTOUT	-
-	-	-	-	-	39	E8	PC8	I/O	FT	-	TIM3_CH3, TSC_G4_IO3, EVENTOUT	-
-	-	-	-	-	40	D8	PC9	I/O	FT	-	TIM3_CH4, TSC_G4_IO4, EVENTOUT	-
14	E2	18	29	29	41	D7	PA8	I/O	FT	-	MCO, TIM1_CH1, MCO2, USART1_CK, TSC_G7_IO1, LPTIM2_CH1, EVENTOUT	-

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP27	UFQFPN32	LQFP48	UFQFPN48	LQFP64	UFBGA64						
14	D3	19	30	30	42	C7	PA9	I/O	FT_fa	-	MCO, TIM1_CH2, I2C1_SCL, I2C2_SCL, USART1_TX, TSC_G7_IO2, TIM15_BKIN, EVENTOUT	COMP1_INP4
14	D1	20	31	31	43	C6	PA10	I/O	FT_f	-	TIM1_CH3, MCO2, I2C1_SDA, I2C2_SDA, SPI2_NSS, USART1_RX, TSC_G7_IO3, EVENTOUT	-
15	C4	21	32	32	44	C8	PA11 [PA9]	I/O	FT	(3)	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, SPI2_MISO, USART1_CTS, COMP1_OUT, EVENTOUT	-
16	B5	22	33	33	45	B8	PA12 [PA10]	I/O	FT	(3)	TIM1_ETR, SPI1_MOSI, SPI2_MOSI, USART1_RTS/USART1_DE, EVENTOUT	-
17	C2	23	34	34	46	A8	PA13 (SWDIO)	I/O	FT	(4)	SWDIO, IR_OUT, TSC_G7_IO4, EVENTOUT	-
-	-	-	35	35	47	D5	VSS	S	-	-	-	-
-	-	-	36	36	48	E4	VDD	S	-	-	-	-
18	B1	24	37	37	49	A7	PA14 (SWCLK)	I/O	FT	(4)	SWCLK, LPTIM1_CH1, TSC_G3_IO4, EVENTOUT	-
-	-	-	-	-	-	E5	VDD	S	-	-	-	-
-	-	25	38	38	50	A6	PA15	I/O	FT	-	TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, USART3_RTS/USART3_DE, USART4_RTS/USART4_DE, TSC_G3_IO1, EVENTOUT	-
-	-	-	-	-	51	B7	PC10	I/O	FT	-	USART3_TX, USART4_TX, TSC_G3_IO2, EVENTOUT	-
-	-	-	-	-	52	B6	PC11	I/O	FT	-	USART3_RX, USART4_RX, TSC_G3_IO3, EVENTOUT	-
-	-	-	-	-	53	C5	PC12	I/O	FT	-	USART3_CK, USART4_CK, EVENTOUT	-
-	-	-	-	-	54	B5	PD2	I/O	FT	-	TIM3_ETR, USART3_RTS/USART3_DE, TSC_SYNC, EVENTOUT	-
-	-	26	39	39	55	A5	PB3	I/O	FT_fa	-	TIM2_CH2, LPTIM1_CH3, I2C2_SCL, I2C3_SCL, SPI1_SCK, USART1_RTS/ USART1_DE, EVENTOUT	-
18	-	27	40	40	56	A4	PB4	I/O	FT_f	-	LPTIM1_CH4, TIM3_CH1, I2C2_SDA, I2C3_SDA, SPI1_MISO, USART1_CTS, TSC_G2_IO1, EVENTOUT	-
18	B3	28	41	41	57	C4	PB5	I/O	FT	-	LPTIM1_IN1, TIM3_CH2, SPI1_MOSI, USART1_CK, TSC_G2_IO2, TIM16_BKIN, EVENTOUT	-
18	A2	29	42	42	58	D3	PB6	I/O	FT_f	-	LPTIM1_ETR, I2C1_SCL, I2C2_SCL, USART1_TX, TSC_G2_IO3, LPUART2_TX, TIM16_CH1N, EVENTOUT	-

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP27	UFQFPN32	LQFP48	UFQFPN48	LQFP64	UFBGA64						
19	A4	30	43	43	59	C3	PB7	I/O	FT_fa	-	LPTIM1_IN2, I2C1_SDA, I2C2_SDA, USART1_RX, USART4_CTS, TSC_G2_IO4, LPUART2_RX, EVENTOUT	-
20	A6	31	44	44	60	B4	PF3-BOOT0 (BOOT0)	I/O	FT	-	EVENTOUT	-
1	-	-	45	45	61	B3	PB8	I/O	FT_f	-	LPTIM1_IN2, I2C2_SCL, I2C1_SCL, USART3_TX, TIM16_CH1, EVENTOUT	-
1	-	-	46	46	62	A3	PB9	I/O	FT_f	-	IR_OUT, I2C2_SDA, I2C1_SDA, SPI2_NSS, USART3_RX, LPTIM1_CH4, EVENTOUT	-
2	-	32	47	47	63	D4	VSS	S	-	-	-	-
3	-	1	48	48	64	E4	VDD	S	-	-	-	-
-	-	-	48	48	64	E4	VDD	S	-	-	-	-

1. *PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:*
   - *The speed should not exceed 2 MHz with a maximum load of 30 pF*
   - *These GPIOs must not be used as current sources (for example to drive a LED).*
2. *After an RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers. The RTC registers are not reset upon system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the RM0503 reference manual.*
3. *Pins PA9/PA10 can be remapped in place of pins PA11/PA12 (default mapping), using SYSCFG_CFGR1 register.*
4. *Upon reset, these pins are configured as SW debug alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.*

4.3 Alternate functions

Table 13. Port A alternate functions

Port A		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/TIM1/2	LPTIM1/ TIM1/2/3	I2C2/SYS_AF/ USART2	I2C1/2/3	I2C2/SPI1/2	COMP1/SPI2	USART1/2/3	LPUART1/2/ USART4	TSC	LPUART2	-	COMP1	-	LPTIM1/2/ TIM2/15/16	EVENTOUT
Port A	PA0	-	TIM2_CH1	-	-	-	-	-	USART2_CTS	USART4_TX	-	-	-	COMP1_OUT	-	TIM2_ETR	EVENTOUT
	PA1	-	TIM2_CH2	LPTIM1_CH2	-	-	SPI1_SCK	SPI2_SCK	USART2_RTS/ USART2_DE	USART4_RX	-	-	-	-	-	TIM15_CH1N	EVENTOUT
	PA2	-	TIM2_CH3	-	-	-	-	-	USART2_TX	LPUART1_TX	-	-	-	-	-	TIM15_CH1	EVENTOUT
	PA3	-	TIM2_CH4	-	-	-	-	-	USART2_RX	LPUART1_RX	-	-	-	-	-	TIM15_CH2	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	-	LPTIM2_CH1	EVENTOUT
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	USART3_TX	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	I2C2_SDA	I2C3_SDA	SPI1_MISO	COMP1_OUT	USART3_CTS	LPUART1_CTS	TSC_G5_IO1	-	-	-	-	TIM16_CH1	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	I2C2_SCL	I2C3_SCL	SPI1_MOSI	-	USART3_RX	-	-	-	-	-	-	LPTIM2_CH2	EVENTOUT
	PA8	MCO	TIM1_CH1	-	MCO2	-	-	-	USART1_CK	-	TSC_G7_IO1	-	-	-	-	LPTIM2_CH1	EVENTOUT
	PA9	MCO	TIM1_CH2	-	-	I2C1_SCL	I2C2_SCL	-	USART1_TX	-	TSC_G7_IO2	-	-	-	-	TIM15_BKIN	EVENTOUT
	PA10	-	TIM1_CH3	-	MCO2	I2C1_SDA	I2C2_SDA	SPI2_NSS	USART1_RX	-	TSC_G7_IO3	-	-	-	-	-	EVENTOUT
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	SPI2_MISO	USART1_CTS	-	-	-	-	COMP1_OUT	-	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	SPI2_MOSI	USART1_RTS/ USART1_DE	-	-	-	-	-	-	-	EVENTOUT
	PA13	SWDIO	IR_OUT	-	-	-	-	-	-	-	TSC_G7_IO4	-	-	-	-	-	EVENTOUT
	PA14	SWCLK	LPTIM1_CH1	-	-	-	-	-	-	-	TSC_G3_IO4	-	-	-	-	-	EVENTOUT
	PA15	-	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	-	USART3_RTS/ USART3_DE	USART4_RTS/ USART4_DE	TSC_G3_IO1	-	-	-	-	-	EVENTOUT

Table 14. Port B alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/ TIM1/2	LPTIM1/ TIM1/2/3	I2C2/ SYS_AF/ USART2	I2C1/2/3	I2C2/SPI1/2	COMP1/ SPI2	USART1/2/3	LPUART1/2/ USART4	TSC	LPUART2	-	COMP1	-	LPTIM1/2/ TIM2/15/16	EVENTOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	-	-	SPI1_NSS	-	USART3_CK	LPUART2_CTS	TSC_G5_IO2	-	-	COMP1_OUT	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	-	-	-	-	USART3_RTS/ USART3_DE	LPUART1_RTS/ LPUART1_DE	TSC_SYNC	LPUART2_RTS/ LPUART2_DE	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	RTC_OUT2	LPTIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	-	TIM2_CH2	LPTIM1_CH3	I2C2_SCL	I2C3_SCL	SPI1_SCK	-	USART1_RTS/ USART1_DE	-	-	-	-	-	-	-	EVENTOUT
	PB4	-	LPTIM1_CH4	TIM3_CH1	I2C2_SDA	I2C3_SDA	SPI1_MISO	-	USART1_CTS	-	TSC_G2_IO1	-	-	-	-	-	EVENTOUT
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	-	SPI1_MOSI	-	USART1_CK	-	TSC_G2_IO2	-	-	-	-	TIM16_BKIN	EVENTOUT
	PB6	-	LPTIM1_ETR	-	-	I2C1_SCL	I2C2_SCL	-	USART1_TX	-	TSC_G2_IO3	LPUART2_TX	-	-	-	TIM16_CH1N	EVENTOUT
	PB7	-	LPTIM1_IN2	-	-	I2C1_SDA	I2C2_SDA	-	USART1_RX	USART4_CTS	TSC_G2_IO4	LPUART2_RX	-	-	-	-	EVENTOUT

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/ TIM1/2	LPTIM1/ TIM1/2/3	I2C2/ SYS_AF/ USART2	I2C1/2/3	I2C2/SPI1/2	COMP1/ SPI2	USART1/2/3	LPUART1/2/ USART4	TSC	LPUART2	-	COMP1	-	LPTIM1/2/ TIM2/15/16	EVENTOUT
Port B	PB8	-	LPTIM1_IN2	-	I2C2_SCL	I2C1_SCL	-	-	USART3_TX	-	-	-	-	-	-	TIM16_CH1	EVENTOUT
	PB9	-	IR_OUT	-	I2C2_SDA	I2C1_SDA	SPI2_NSS	-	USART3_RX	-	-	-	-	-	-	LPTIM1_CH4	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK	-	USART3_TX	LPUART1_RX	TSC_G5_IO3	LPUART2_RX	-	COMP1_OUT	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	LPUART1_TX	TSC_G5_IO4	LPUART2_TX	-	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	-	SPI2_NSS	-	USART3_CK	LPUART1_RTS/ LPUART1_DE	TSC_G1_IO1	-	-	-	-	TIM15_BKIN	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	-	USART3_CTS	LPUART1_CTS	TSC_G1_IO2	-	-	-	-	TIM15_CH1N	EVENTOUT
	PB14	-	TIM1_CH2N	-	-	I2C2_SDA	SPI2_MISO	-	USART3_RTS/ USART3_DE	-	TSC_G1_IO3	-	-	-	-	TIM15_CH1	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	-	-	SPI2_MOSI	-	-	-	TSC_G1_IO4	-	-	-	-	TIM15_CH2	EVENTOUT

Table 15. Port C alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/SYS_AF/ TIM1/2	LPTIM1/TIM1/2/3	I2C2/ SYS_AF/ USART2	I2C1/2/3	I2C2/SPI1/2	COMP1/SPI2	USART1/2/3	LPUART1/2/ USART4	TSC	LPUART2	-	COMP1	-	LPTIM1/2/ TIM2/15/16	EVENTOUT
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	-	-	LPUART1_RX	-	LPUART2_TX	-	-	-	LPTIM2_IN1	EVENTOUT
	PC1	-	LPTIM1_CH1	-	-	I2C3_SDA	-	-	-	LPUART1_TX	-	LPUART2_RX	-	-	-	-	EVENTOUT
	PC2	MCO2	LPTIM1_IN2	-	-	-	SPI2_MISO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI	-	-	USART4_CK	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PC4	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	-	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	-	-	-	-	-	LPUART2_TX	TSC_G4_IO1	-	-	-	-	-	EVENTOUT
	PC7	-	-	TIM3_CH2	-	-	-	-	-	LPUART2_RX	TSC_G4_IO2	-	-	-	-	LPTIM2_CH2	EVENTOUT
	PC8	-	-	TIM3_CH3	-	-	-	-	-	-	TSC_G4_IO3	-	-	-	-	-	EVENTOUT
	PC9	-	-	TIM3_CH4	-	-	-	-	-	-	TSC_G4_IO4	-	-	-	-	-	EVENTOUT
	PC10	-	-	-	-	-	-	-	USART3_TX	USART4_TX	TSC_G3_IO2	-	-	-	-	-	EVENTOUT
	PC11	-	-	-	-	-	-	-	USART3_RX	USART4_RX	TSC_G3_IO3	-	-	-	-	-	EVENTOUT
	PC12	-	-	-	-	-	-	-	USART3_CK	USART4_CK	-	-	-	-	-	-	EVENTOUT
	PC13	-	-	LPTIM1_CH3	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	OSC32_EN	OSC_EN	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 16. Port D alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/SYS_AF/ TIM1/2	LPTIM1/TIM1/2/3	I2C2/SYS_AF/ USART2	I2C1/2/3	I2C2/ SPI1/2	COMP1/SPI2	USART1/2/3	LPUART1/2/ USART4	TSC	LPUART2	-	COMP1	-	LPTIM1/2/ TIM2/15/16	EVENTOUT
Port D	PD2	-	-	TIM3_ETR	-	--		-	USART3_RTS/ USART3_DE	-	TSC_SYNC	-	-	-	-	-	EVENTOUT

Table 17. Port F alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/SYS_AF/ TIM1/2	LPTIM1/TIM1/2/3	I2C2/SYS_AF/USART2	I2C1/2/3	I2C2/SPI1/2	COMP1/SPI2	USART1/2/3	LPUART1/2/USART4	TSC	LPUART2	-	COMP1	-	LPTIM1/2/TIM2/15/16	EVENTOUT
Port F	PF0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PF1	OSC_EN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PF2	MCO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

5 Memory mapping

Refer to the product line reference manual (RM0503) for details on the memory mapping as well as the boundary addresses for all peripherals.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an junction temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} =V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 10.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 11.

Figure 10. Pin loading conditions

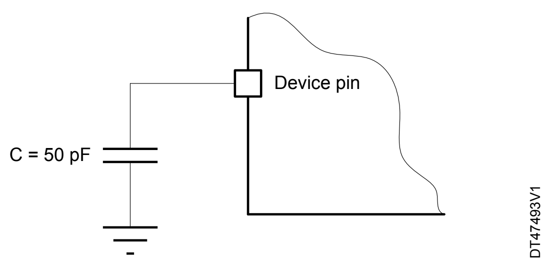
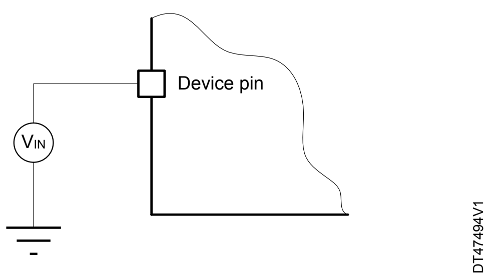
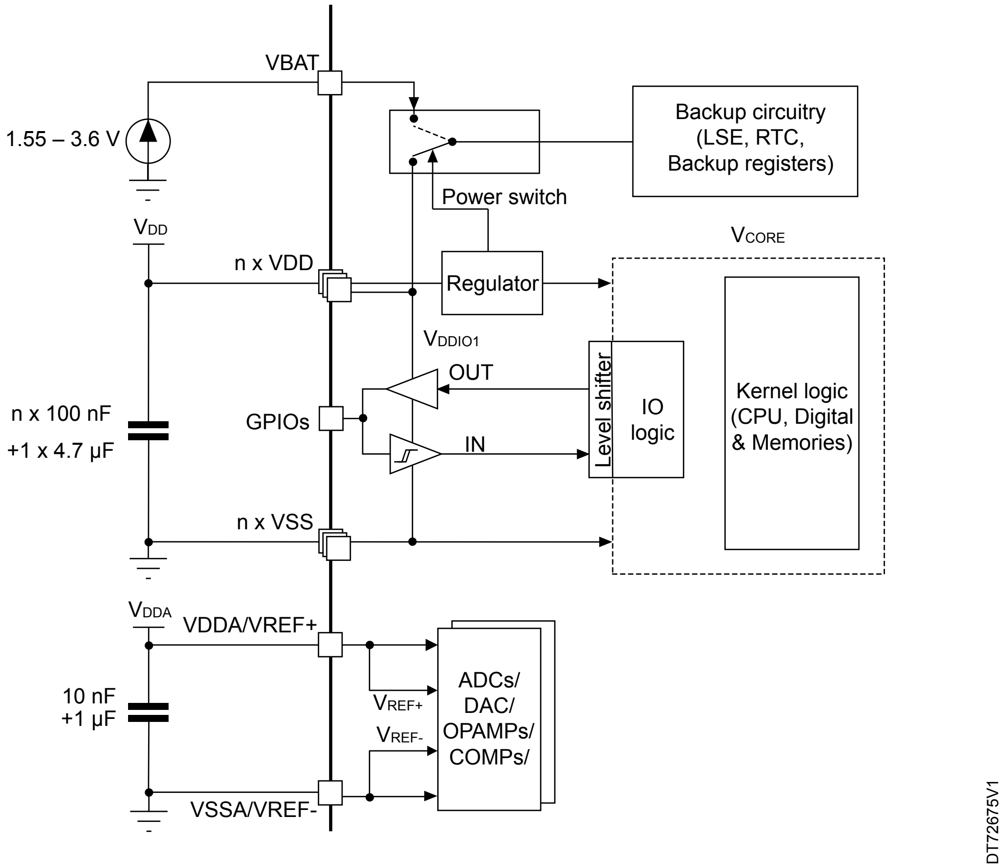


Figure 11. Pin input voltage



6.1.6 Power supply scheme

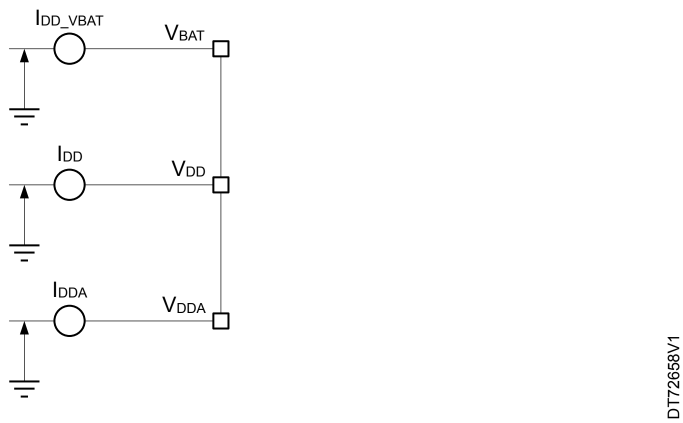
Figure 12. Power supply scheme



Caution: Each power supply pair (such as V_{DD}/V_{SS}, V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



The I_{DD_ALL} parameters given in Table 25. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, bypass mode, ART enabled (cache ON, prefetch OFF), HSE clock used as system clock to Table 42. Current consumption in VBAT mode represent the total MCU consumption including the current supplying V_{DD}, V_{DDA}, and V_{BAT}.

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 18. Voltage characteristics, Table 19. Current characteristics and Table 20. Thermal characteristics may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 18. Voltage characteristics

All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Symbol	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD}, V_{DDA}, V_{BAT})	-0.3	4.0	V
V_{IN}[(1)]	Input voltage on FT_xxx pins	V_{SS} - 0.3	min (V_{DD}, V_{DDA}) + 4.0[(2)(3)]	V
	Input voltage on TT_xx pins	V_{SS} - 0.3	4.0	
	Input voltage on any other pins	V_{SS} - 0.3	4.0	
$\|\Delta V_{DDX}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins[(4)]	-	50	mV

1. *V_{IN} maximum must always be respected. Refer to Table 19. Current characteristics for the maximum allowed injected current values.*
2. *To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.*
3. *This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.*
4. *Including VREF- pin.*

Table 19. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)[(1)]	140	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)	140	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins[(2)]	100	
	Total output current sourced by sum of all I/Os and control pins[(2)]	100	
$I_{INJ(PIN)}$[(3)]	Injected current on FT_xxx, TT_xx, RST	-5/+0[(4)]	
$\sum \|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)	25	

1. *All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.*
2. *This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.*
3. *Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.*
4. *A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to Table 18. Voltage characteristics for the maximum allowed input voltage values.*

5. *When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).*

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	56	MHz
f_{PCLK}	Internal APB clock frequency	-	0	56	
V_{DD}	Standard operating voltage	-	1.71[1]	3.6	V
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		OPAMP used	1.8		
		ADC, OPAMP, COMP not used	0		
V_{BAT}	Backup domain supply voltage	-	1.55	3.6	
V_{IN}	I/O input voltage	TT_xx I/Os	-0.3	V_{DDIOx} + 0.3	V
		All I/Os except TT_xx pins	-0.3	Min(Min(V_{DD}, V_{DDA}) + 3.6, 5.5)[2][3]	
T_A	Ambient temperature for suffix 6	Maximum power dissipation	-40	85	°C
		Low-power dissipation[4]		105	
	Ambient temperature for suffix 3	Maximum power dissipation		125	
		Low-power dissipation[4]		130	
T_J	Junction temperature range	Suffix 6 version	-40	105	
		Suffix 3 version		130	

1. *When RESET is released, the functionality is guaranteed down to V_{BOR0} min.*
2. *This formula has to be applied only on the power supplies related to the I/O structure described by the pin definition table. The maximum I/O input voltage is the smallest value between Min (V_{DD}, V_{DDA}) + 3.6 V and 5.5 V.*
3. *For operation with voltage higher than Min (V_{DD}, V_{DDA}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled.*
4. *In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_J max (see Section 7.9: Package thermal characteristics).*

6.3.2 Operating conditions at power-up / power-down

The parameters given in Table 22 are derived from tests performed under the ambient temperature condition summarized in Section 6.3.1: General operating conditions.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate	ULPEN = 0	10	∞	µs/V
		ULPEN = 1	100	∞	ms/V
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate	-	10	∞	µs/V

6.3.3 Embedded reset and power control block characteristics

The parameters given in Table 23. Embedded reset and power control block characteristics are derived from tests performed under the ambient temperature conditions summarized in Section 6.3.1: General operating conditions.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brownout reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	V
V_{BOR1}	Brownout reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	V
V_{BOR2}	Brownout reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	V
V_{BOR3}	Brownout reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	V
V_{BOR4}	Brownout reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	V
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	V
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	V
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	V
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	V
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	V
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	V
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	V
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	mV

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)[2]	BOR (except BOR0) and PVD consumption from V_{DD}[3]	-	-	1.1	1.6	µA
	BOR[3] (except BOR0) and PVD average consumption from V_{DD} with ENULP = 1	-	-	55	1000	nA
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1)[2]	PVM1 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4)[2]	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. *Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.*
2. *Specified by design, not tested in production.*
3. *BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.*

6.3.4 Embedded voltage reference

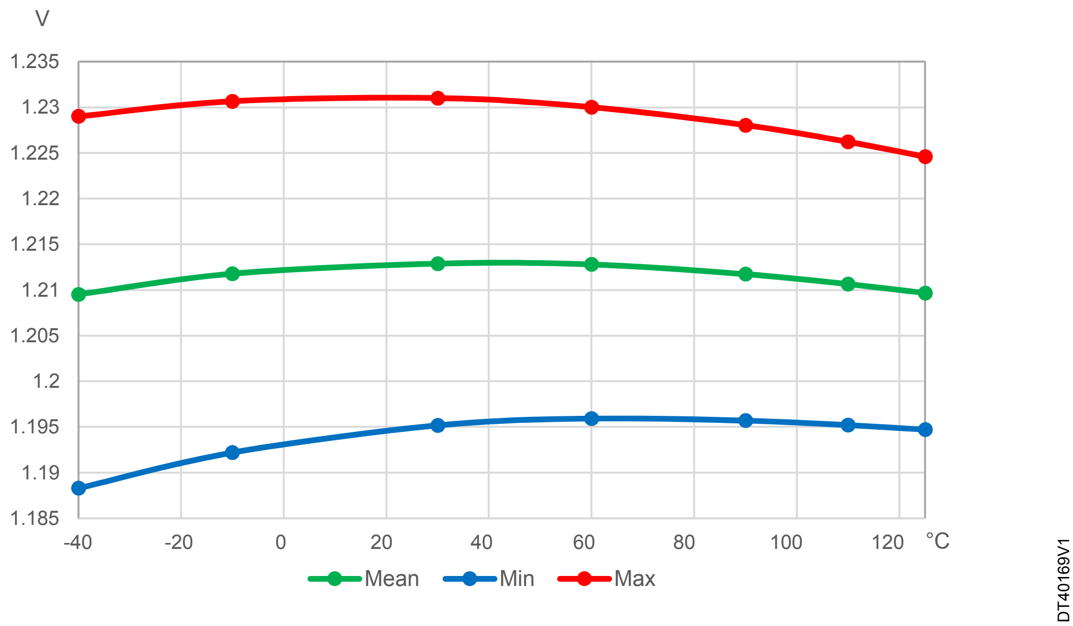
The parameters given in Table 24. Embedded internal voltage reference are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Table 24. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$[1]	ADC sampling time when reading the internal reference voltage	-	4[2]	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12[2]	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20[2]	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5[2]	mV
T_{Coeff}	Temperature coefficient	-40°C < T_A < +130°C	-	30	50[2]	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000[2]	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200[2]	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. *The shortest sampling time can be determined in the application by multiple iterations.*
2. *Specified by design, not tested in production.*

Figure 14. V_{REFINT} versus temperature



6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Figure 13. Current consumption measurement scheme.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table "Number of wait states according to CPU clock (HCLK) frequency" available in the RM0503 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in Table 25 to Table 42 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Table 25. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, bypass mode, ART enabled (cache ON, prefetch OFF), HSE clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max(1)					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$, bypass mode, peripherals disabled	Range 1	48 MHz	3.75	3.75	3.80	3.85	4.00	4.1	4.15	4.25	4.4	4.65	mA
				32 MHz	2.55	2.55	2.60	2.65	2.80	2.8	2.85	2.9	3.05	3.3	
				24 MHz	1.95	1.95	2.00	2.05	2.15	2.15	2.15	2.25	2.35	2.6	
				16 MHz	1.35	1.35	1.40	1.45	1.55	1.45	1.5	1.55	1.7	1.9	
			Range 2	16 MHz	1.10	1.15	1.15	1.20	1.30	1.25	1.25	1.3	1.4	1.65	
				8 MHz	0.615	0.625	0.655	0.700	0.795	0.68	0.7	0.755	0.85	1.055	
				4 MHz	0.360	0.375	0.395	0.440	0.535	0.4	0.415	0.465	0.56	0.76	
				2 MHz	0.235	0.240	0.265	0.310	0.405	0.26	0.275	0.325	0.41	0.615	
				1 MHz	0.170	0.180	0.200	0.245	0.345	0.19	0.2	0.25	0.34	0.54	
				400 kHz	0.135	0.145	0.165	0.205	0.300	0.145	0.16	0.205	0.295	0.495	
				100 kHz	0.115	0.120	0.145	0.185	0.280	0.125	0.14	0.185	0.275	0.475	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.160	0.165	0.200	0.235	0.340	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.085	0.090	0.115	0.160	0.265	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.040	0.045	0.070	0.120	0.220	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.020	0.025	0.055	0.095	0.200	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, ART enabled (cache ON, prefetch OFF), MSI clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max(1)					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	Range 1	48 MHz	3.75	3.80	3.90	4.00	4.15	4.1	4.25	4.45	4.6	4.95	mA
				32 MHz	2.55	2.60	2.65	2.75	2.90	2.8	2.9	3	3.2	3.5	
				24 MHz	1.95	2.00	2.05	2.10	2.25	2.15	2.2	2.35	2.5	2.8	
				16 MHz	1.35	1.35	1.40	1.50	1.60	1.45	1.55	1.6	1.75	2.05	
			Range 2	16 MHz	1.10	1.15	1.20	1.25	1.35	1.25	1.3	1.35	1.5	1.75	
				8 MHz	0.605	0.615	0.650	0.705	0.815	0.735	0.755	0.765	0.865	1.1	
				4 MHz	0.355	0.365	0.395	0.445	0.555	0.435	0.44	0.475	0.575	0.81	
				2 MHz	0.235	0.245	0.270	0.315	0.430	0.295	0.305	0.34	0.43	0.66	
				1 MHz	0.170	0.190	0.205	0.255	0.365	0.23	0.235	0.275	0.36	0.585	
				400 kHz	0.135	0.145	0.165	0.215	0.320	0.19	0.2	0.24	0.31	0.54	
				100 kHz	0.115	0.120	0.145	0.195	0.305	0.17	0.18	0.235	0.29	0.52	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.155	0.165	0.195	0.245	0.360	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.085	0.095	0.120	0.170	0.290	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.045	0.045	0.075	0.125	0.245	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.020	0.025	0.055	0.105	0.220	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

Table 27. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, bypass mode, ART disabled (cache ON, prefetch OFF), HSE clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max[1]					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$, bypass mode , peripherals disabled	Range 1	48 MHz	4.05	4.05	4.15	4.20	4.35	4.45	4.5	4.65	4.85	5.1	mA
				32 MHz	2.75	2.80	2.85	2.90	3.05	3.05	3.1	3.2	3.35	3.6	
				24 MHz	2.40	2.40	2.45	2.50	2.65	2.6	2.65	2.8	2.9	3.2	
				16 MHz	1.65	1.65	1.70	1.75	1.90	1.8	1.85	1.95	2.05	2.3	
			Range 2	16 MHz	1.20	1.20	1.25	1.30	1.40	1.3	1.35	1.4	1.5	1.75	
				8 MHz	0.730	0.745	0.775	0.820	0.920	0.805	0.83	0.89	0.985	1.2	
				4 MHz	0.420	0.430	0.455	0.500	0.595	0.46	0.48	0.535	0.625	0.83	
				2 MHz	0.265	0.270	0.295	0.340	0.435	0.29	0.305	0.355	0.445	0.65	
				1 MHz	0.185	0.195	0.215	0.260	0.355	0.205	0.22	0.27	0.355	0.555	
				400 kHz	0.140	0.145	0.170	0.210	0.310	0.15	0.165	0.215	0.3	0.505	
				100 kHz	0.115	0.120	0.145	0.190	0.285	0.125	0.14	0.19	0.275	0.475	
$I_{DD (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.195	0.200	0.230	0.275	0.375	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.105	0.110	0.135	0.180	0.285	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.050	0.055	0.090	0.125	0.230	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.020	0.025	0.050	0.100	0.200	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, bypass mode, ART disabled (cache ON, prefetch OFF), MSI clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max[1]					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	Range 1	48 MHz	4.05	4.10	4.25	4.35	4.50	4.45	4.6	4.85	5.05	5.45	mA
				32 MHz	2.75	2.80	2.90	3.00	3.15	3.1	3.15	3.3	3.5	3.85	
				24 MHz	2.35	2.45	2.50	2.60	2.75	3	3.05	3.05	3.05	3.4	
				16 MHz	1.65	1.70	1.75	1.80	1.95	1.8	1.9	2	2.15	2.45	
			Range 2	16 MHz	1.20	1.20	1.25	1.30	1.45	1.3	1.35	1.45	1.6	1.85	
				8 MHz	0.720	0.735	0.765	0.820	0.945	0.95	1	1	1	1.25	
				4 MHz	0.415	0.425	0.455	0.505	0.620	0.49	0.5	0.54	0.645	0.85	
				2 MHz	0.260	0.270	0.300	0.350	0.460	0.335	0.345	0.4	0.465	0.7	
				1 MHz	0.185	0.195	0.220	0.270	0.380	0.255	0.26	0.295	0.375	0.65	
				400 kHz	0.140	0.145	0.170	0.220	0.330	0.195	0.2	0.24	0.32	0.6	
				100 kHz	0.115	0.125	0.150	0.195	0.305	0.175	0.185	0.225	0.29	0.6	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.190	0.200	0.235	0.285	0.405	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.105	0.110	0.140	0.190	0.310	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.045	0.055	0.080	0.135	0.250	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.020	0.030	0.055	0.105	0.225	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

Table 29. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, bypass mode, HSE clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max[1]					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$, bypass mode , peripherals disabled	Range 1	48 MHz	3.40	3.40	3.45	3.55	3.65	3.7	3.8	3.9	4.05	4.3	mA
				32 MHz	2.30	2.35	2.35	2.45	2.55	2.5	2.6	2.65	2.8	3.05	
				24 MHz	1.75	1.80	1.80	1.90	2.00	1.95	1.95	2.05	2.2	2.45	
				16 MHz	1.20	1.25	1.25	1.30	1.45	1.35	1.35	1.45	1.55	1.8	
			Range 2	16 MHz	1.00	1.05	1.05	1.10	1.20	1.1	1.15	1.2	1.3	1.55	
				8 MHz	0.565	0.575	0.605	0.650	0.750	0.62	0.645	0.7	0.795	1	
				4 MHz	0.335	0.345	0.375	0.415	0.510	0.37	0.385	0.44	0.53	0.735	
				2 MHz	0.225	0.235	0.255	0.295	0.395	0.245	0.26	0.31	0.4	0.6	
				1 MHz	0.165	0.170	0.195	0.240	0.335	0.18	0.195	0.245	0.335	0.535	
				400 kHz	0.130	0.140	0.160	0.205	0.300	0.145	0.16	0.205	0.295	0.495	
				100 kHz	0.115	0.120	0.145	0.185	0.280	0.125	0.135	0.185	0.275	0.475	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.069	0.075	0.100	0.140	0.255	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.037	0.044	0.068	0.115	0.215	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.018	0.024	0.049	0.095	0.200	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.008	0.015	0.040	0.085	0.190	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

Table 30. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, MSI clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max[1]					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	Range 1	48 MHz	3.35	3.45	3.50	3.60	3.80	3.7	3.85	4	4.2	4.55	mA
				32 MHz	2.30	2.35	2.40	2.50	2.65	2.5	2.6	2.75	2.95	3.25	
				24 MHz	1.75	1.80	1.85	1.90	2.05	1.95	2	2.1	2.3	2.6	
				16 MHz	1.20	1.25	1.30	1.35	1.50	1.35	1.4	1.5	1.65	1.9	
			Range 2	16 MHz	1.00	1.05	1.10	1.15	1.25	1.15	1.15	1.25	1.4	1.65	
				8 MHz	0.550	0.565	0.595	0.645	0.760	0.65	0.7	0.695	0.805	1.045	
				4 MHz	0.330	0.340	0.370	0.420	0.530	0.41	0.45	0.44	0.545	0.78	
				2 MHz	0.220	0.235	0.255	0.305	0.415	0.29	0.29	0.32	0.42	0.65	
				1 MHz	0.165	0.170	0.200	0.250	0.360	0.225	0.23	0.27	0.355	0.58	
				400 kHz	0.130	0.140	0.165	0.210	0.320	0.18	0.195	0.24	0.31	0.535	
				100 kHz	0.115	0.120	0.145	0.195	0.305	0.165	0.18	0.23	0.29	0.52	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.068	0.075	0.100	0.155	0.275	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.038	0.045	0.072	0.125	0.240	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.018	0.024	0.051	0.105	0.220	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.009	0.015	0.042	0.095	0.210	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

Table 31. Typical current consumption in Run and Low-power run modes, with different codes running from flash memory, ART enabled (cache ON, prefetch OFF)

Symbol	Parameter	Conditions			Typical consumption				Typical consumption				Typical consumption			
		Clock source	Range	Code	25 °C, 1.8 V				25 °C, 3.0 V				25 °C, 3.6 V			
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disabled	Range 1, 48 MHz	Coremark	3610	μA	75	μA/MHz	3750	μA	78	μA/MHz	3790	μA	79	μA/MHz
				Reduced code	3780		79		3930		82		3970		83	
				Dhrystone 2.1	3560		74		3710		77		3750		78	
				Fibonacci	3630		76		3770		79		3800		79	
				While(1)	2500		52		2600		54		2630		55	
			Range 2, 16 MHz	Coremark	1080		68		1120		70		1130		71	
				Reduced code	1130		71		1180		74		1190		74	
				Dhrystone 2.1	1080		68		1120		70		1130		71	

Symbol	Parameter	Conditions			Typical consumption 25 °C, 1.8 V				Typical consumption 25 °C, 3.0 V				Typical consumption 25 °C, 3.6 V			
		Clock source	Range	Code												
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disabled	Range 2, 16 MHz	Fibonacci	1090	µA	68	µA/ MHz	1120	µA	70	µA/ MHz	1140	µA	71	µA/ MHz
				While(1)	780		49		810		51		820		51	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run, 2 MHz	Coremark	150		75		160		80		160		80	
				Reduced code	160		80		160		80		160		80	
				Dhrystone 2.1	150		75		150		75		160		80	
				Fibonacci	150		75		160		80		160		80	
				While(1)	110		55		110		55		110		55	

Table 32. Typical current consumption in Run and Low-power run modes, with different codes running from flash memory, ART disabled

Symbol	Parameter	Conditions			Typical consumption 25 °C, 1.8 V				Typical consumption 25 °C, 3.0 V				Typical consumption 25 °C, 3.6 V			
		Clock source	Range	Code												
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disabled	Range 1, 48 MHz	Coremark	3870	µA	81	µA/ MHz	4040	µA	84	µA/ MHz	4090	µA	85	µA/ MHz
				Reduced code	4010		84		4180		87		4220		88	
				Dhrystone 2.1	3870		81		4030		84		4080		85	
				Fibonacci	3930		82		4110		86		4160		87	
				While(1)	2500		52		2600		54		2630		55	
			Range 2, 16 MHz	Coremark	1150		72		1190		74		1210		76	
				Reduced code	1190		74		1240		78		1260		79	
				Dhrystone 2.1	1150		72		1200		75		1210		76	
				Fibonacci	1160		73		1210		76		1230		77	
				While(1)	780		49		810		51		820		51	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run, 2 MHz	Coremark	190		95		190		95		190		95	
				Reduced code	190		95		200		100		200		100	
				Dhrystone 2.1	190		95		190		95		190		95	
				Fibonacci	200		100		210		105		210		105	
				While(1)	110		55		110		55		110		55	

Table 33. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions			Typical consumption 25 °C, 1.8 V				Typical consumption 25 °C, 3.0 V				Typical consumption 25 °C, 3.6 V			
		Clock source	Range	Code												
$I_{DD (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disabled	Range 1, 48 MHz	Coremark	3250	µA	68	µA/ MHz	3370	µA	70	µA/ MHz	3410	µA	71	µA/ MHz
				Reduced code	3300		69		3430		71		3460		72	
				Dhrystone 2.1	3190		66		3310		69		3350		70	
				Fibonacci	3450		72		3590		75		3630		76	
				While(1)	2660		55		2760		58		2790		58	
			Range 2, 16 MHz	Coremark	980		61		1020		64		1030		64	
				Reduced code	1000		63		1040		65		1050		66	
				Dhrystone 2.1	970		61		1000		63		1010		63	
				Fibonacci	1030		64		1070		67		1080		68	
				While(1)	830		52		860		54		860		54	
$I_{DD (LPRun)}$	Supply current in Low-power run mode		Low-power run, 2 MHz	Coremark	130		65		130		65		130		65	
				Reduced code	130		65		140		70		140		70	
				Dhrystone 2.1	130		65		130		65		130		65	
				Fibonacci	140		70		140		70		140		70	
				While(1)	110		55		110		55		110		55	

Table 34. Current consumption in Sleep and Low-power sleep modes, flash memory ON, HSE clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			TYP					MAX (DS rounded)					Unit
				f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD (Sleep)}$	Supply current in Sleep mode	$f_{HCLK} = f_{HSE}$, peripherals disabled	Range 1	48 MHz	1.15	1.2	1.2	1.3	1.4	1.3	1.3	1.4	1.5	1.75	mA
				32 MHz	0.83	0.845	0.8	0.95	1.05	0.905	0.935	1	1.1	1.35	
				24 MHz	0.65	0.665	0.695	0.745	0.86	0.71	0.74	0.805	0.915	1.15	
				16 MHz	0.475	0.485	0.52	0.57	0.69	0.525	0.545	0.61	0.715	0.945	
			Range 2	16 MHz	0.42	0.425	0.455	0.5	0.6	0.46	0.48	0.53	0.63	0.835	
				8 MHz	0.265	0.275	0.295	0.34	0.44	0.29	0.31	0.36	0.45	0.655	
				4 MHz	0.185	0.195	0.22	0.26	0.36	0.205	0.22	0.27	0.36	0.56	
				2 MHz	0.145	0.155	0.18	0.22	0.32	0.16	0.175	0.225	0.315	0.515	
				1 MHz	0.13	0.135	0.16	0.2	0.295	0.14	0.155	0.205	0.29	0.49	
				400 kHz	0.115	0.125	0.145	0.19	0.285	0.125	0.14	0.19	0.28	0.48	

Symbol	Parameter	Conditions			TYP					MAX (DS rounded)					Unit
				f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Sleep)}$	Supply current in Sleep mode	$f_{HCLK} = f_{HSE}$, peripherals disabled	Range 2	100 kHz	0.11	0.115	0.145	0.185	0.28	0.12	0.135	0.185	0.275	0.475	mA
$I_{DD\ (LPSleep)}$	Supply current in Low-power sleep mode		LP Sleep	2 MHz	0.055	0.062	0.087	0.135	0.235	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.033	0.039	0.065	0.11	0.215	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.02	0.026	0.052	0.1	0.2	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.013	0.02	0.045	0.09	0.195	TBD	TBD	TBD	TBD	TBD	

Table 35. Current consumption in Sleep and Low-power sleep modes, flash memory ON, MSI clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Sleep)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	Range 1	48 MHz	1.15	1.20	1.25	1.35	1.40	1.3	1.35	1.4	1.55	1.8	mA
				32 MHz	0.825	0.845	0.90	0.95	1.05	0.905	0.945	1	1.15	1.4	
				24 MHz	0.650	0.665	0.700	0.750	0.87	0.71	0.745	0.82	0.93	1.15	
				16 MHz	0.480	0.490	0.525	0.575	0.69	0.53	0.55	0.62	0.725	0.96	
			Range 2	16 MHz	0.420	0.430	0.460	0.505	0.605	0.47	0.485	0.545	0.64	0.845	
				8 MHz	0.250	0.260	0.285	0.330	0.425	0.295	0.305	0.345	0.435	0.64	
				4 MHz	0.180	0.190	0.215	0.255	0.355	0.225	0.235	0.27	0.355	0.555	
				2 MHz	0.145	0.155	0.175	0.220	0.315	0.19	0.2	0.24	0.315	0.515	
				1 MHz	0.130	0.135	0.160	0.200	0.300	0.175	0.19	0.235	0.295	0.495	
				400 kHz	0.115	0.120	0.145	0.190	0.285	0.165	0.175	0.22	0.275	0.48	
				100 kHz	0.110	0.115	0.145	0.185	0.290	0.155	0.17	0.22	0.275	0.475	
$I_{DD\ (LPSleep)}$	Supply current in Low-power run mode		Low-power sleep mode	2 MHz	0.054	0.060	0.086	0.135	0.235	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.034	0.040	0.066	0.115	0.215	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.019	0.026	0.051	0.100	0.200	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.013	0.020	0.045	0.090	0.195	TBD	TBD	TBD	TBD	TBD	

Table 36. Current consumption in Sleep and Low-power sleep modes, flash memory in power-down mode

TBD stands for "to be defined".

Symbol	Parameter	Conditions		Typ					Max					Unit
		Clock source	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (LPSleep)}$	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	2 MHz	53.5	60.5	86.0	130	235	TBD	TBD	TBD	TBD	TBD	µA
			1 MHz	33.5	40.5	66.0	110	215	TBD	TBD	TBD	TBD	TBD	

Symbol	Parameter	Conditions		Typ					Max					Unit
		Clock source	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (LPSleep)}$	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	400 kHz	19.5	26.0	51.0	98.0	200	TBD	TBD	TBD	TBD	TBD	µA
			100 kHz	13.5	20.0	45.5	92.0	195	TBD	TBD	TBD	TBD	TBD	

Table 37. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions	Typ					Max					Unit
		V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 0)}$	Supply current in Stop 0 mode, RTC disabled	1.8 V	100	105	130	170	265	250	265	325	430	660	µA
		2.4 V	100	110	130	175	270	255	270	330	435	680	
		3.0 V	105	110	130	175	275	260	275	330	440	690	
		3.3 V	105	110	135	175	275	260	275	335	440	695	
		3.6 V	105	110	135	180	280	265	280	335	445	700	

Table 38. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 1)}$	Supply current in Stop 1 mode, RTC disabled	LCD disabled	EN_ULP = 1	1.8 V	2.00	7.20	29.0	70.0	160	5.05	19.0	72.0	175	400	µA
				2.4 V	2.10	7.20	29.0	71.0	165	5.05	19.0	72.0	175	415	
				3.0 V	2.10	7.20	29.0	71.5	170	5.05	19.0	73.5	180	425	
				3.3 V	2.10	7.80	29.5	71.5	170	5.05	19.0	73.5	180	430	
				3.6 V	2.10	7.90	29.5	72.5	175	5.05	20.0	74.5	180	435	
			EN_ULP = 0	1.8 V	2.00	7.20	29.0	70.5	160	5.05	19.0	72.0	175	395	
				2.4 V	2.10	7.20	29.0	71.0	165	5.05	19.0	72.0	175	415	
				3.0 V	2.10	7.20	29.0	71.5	170	5.05	19.0	73.5	180	425	
				3.3 V	2.10	7.80	29.0	71.5	170	6.05	19.0	73.5	180	430	
				3.6 V	2.10	7.90	29.5	72.5	170	6.05	20.0	74.5	180	430	
	Supply current in Stop 1 mode, RTC enabled	RTC clocked by LSI	EN_ULP = 0, LPCAL = 1	1.8 V	2.30	8.90	33.5	83.5	205	6.00	20.0	83.5	210	515	
				2.4 V	2.40	9.00	33.5	84.5	210	6.00	20.0	83.5	210	520	
				3.0 V	2.50	8.10	34.0	85.5	210	6.00	20.0	85.5	215	530	
				3.3 V	2.60	8.80	34.0	86.0	215	7.00	21.0	85.5	215	535	
				3.6 V	2.65	8.90	34.5	87.0	215	7.05	21.0	86.5	215	540	

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 1)}$	Supply current in Stop 1 mode, RTC enabled	RTC clocked by LSE, bypassed at 32768 Hz	EN_ULP = 0, LPCAL = 1	1.8 V	2.10	7.50	27.5	65.0	140	5.00	19.0	69.0	160	355	µA
				2.4 V	2.20	7.50	27.0	65.5	150	6.00	19.0	69.0	165	375	
				3.0 V	2.30	7.10	27.5	65.5	150	6.00	19.0	70.0	165	380	
				3.3 V	2.30	7.20	27.5	66.0	155	6.00	19.0	70.0	165	385	
				3.6 V	2.35	7.80	28.0	66.5	155	6.05	19.0	70.0	165	390	
			LPCAL = 0	1.8 V	2.30	7.20	27.0	65.0	140	6.00	19.0	69.0	160	355	
				2.4 V	2.40	7.80	27.5	65.0	150	6.00	19.0	69.0	165	375	
				3.0 V	2.60	7.90	27.5	66.0	155	7.00	20.0	70.0	165	385	
				3.3 V	2.60	8.10	28.0	66.5	155	7.00	20.0	70.0	165	385	
				3.6 V	2.75	8.20	28.0	67.0	155	7.05	20.0	70.0	165	390	
		RTC clocked by LSE quartz in low-drive mode	EN_ULP = 0, LPCAL = 0	1.8 V	2.30	8.90	33.0	79	180	5.00	20.0	82.0	195	430	
				2.4 V	2.40	9.00	33.5	79.5	185	6.00	20.0	83.5	200	455	
				3.0 V	2.30	8.20	34.0	80.5	180	6.00	21.0	85.5	200	470	
				3.3 V	2.70	8.90	34.0	81.5	180	7.00	21.0	85.5	205	470	
				3.6 V	2.90	9.00	34.5	82.5	200	7.05	21.0	87.5	205	475	
			EN_ULP = 0, LPCAL = 1	1.8 V	2.20	8.20	32.5	79	175	6.00	20.0	82.0	195	430	
				2.4 V	2.20	8.80	33.5	78.5	180	6.00	20.0	83.5	195	455	
				3.0 V	2.20	8.90	33.5	80	185	6.00	20.0	84.5	200	465	
				3.3 V	2.30	9.00	34.0	81	190	6.00	20.0	85.5	200	465	
				3.6 V	2.45	8.10	34.0	82	185	6.05	20.0	85.5	205	470	
			EN_ULP = 1, LPCAL = 1	1.8 V	2.20	8.20	32.5	79	175	5.00	20.0	82.0	195	430	
				2.4 V	2.20	8.80	33.0	78	180	6.00	20.0	83.5	195	455	
				3.0 V	2.20	8.90	33.5	79.5	185	6.00	20.0	84.5	200	465	
				3.3 V	2.30	9.00	34.0	81	190	6.00	20.0	85.5	200	465	
				3.6 V	2.45	8.10	34.0	82	185	6.05	20.0	85.5	205	470	

Table 39. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 2)}$	Supply current in Stop 2 mode, RTC disabled	-	EN_ULP = 1	1.8 V	515	1650	7400	18000	42500	1300	4150	18500	44500	100500	nA
				2.4 V	535	1800	7750	18500	45000	1350	4450	19500	46500	110000	

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD (Stop 2)}$	Supply current in Stop 2 mode, RTC disabled	-	EN_ULP = 1	3.0 V	560	1950	8150	19500	47000	1400	4900	20500	48500	111000	nA
				3.3 V	580	2050	8400	20000	48500	1450	5150	21000	49500	120000	
				3.6 V	620	2200	8700	20500	50000	1550	5450	21500	50500	120500	
			EN_ULP = 0	1.8 V	575	1650	6700	17000	41500	1450	4100	16500	43000	100500	
				2.4 V	580	1650	6850	17500	44000	1450	4150	17000	44000	110000	
				3.0 V	600	1700	7100	18000	46000	1500	4300	17500	45500	110500	
				3.3 V	610	1750	7200	18500	47500	1500	4350	18000	46500	111000	
				3.6 V	630	1800	7400	19000	48500	1550	4500	18500	47500	120000	
	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI	LSIPREDIV	1.8 V	835	1900	6950	17500	42000	2100	4750	17500	43500	105000	
				2.4 V	915	2000	7200	18000	44500	2300	5000	18000	44500	110000	
				3.0 V	1000	2100	7500	18500	46500	2500	5300	18500	46500	115000	
				3.3 V	1050	2200	7700	19000	47500	2650	5500	19000	47500	120000	
				3.6 V	1100	2300	7900	19500	48500	2800	5700	19500	49000	120000	
		RTC clocked by LSE, bypassed at 32768 Hz	EN_ULP = 0, LPCAL = 1	1.8 V	635	1650	6500	16500	40500	1600	4150	16000	41000	100000	
				2.4 V	680	1700	6750	17000	42000	1700	4300	17000	42500	105000	
				3.0 V	730	1800	6950	17500	44000	1800	4500	17500	43500	110000	
				3.3 V	765	1850	7100	18000	45000	1900	4650	17500	44500	110000	
				3.6 V	810	1900	7250	18500	46000	2000	4800	18000	46000	115000	
			EN_ULP = 0, LPCAL = 0	1.8 V	790	1800	6600	16500	41000	2000	4550	16500	41500	100000	
				2.4 V	910	1950	6950	17000	42500	2250	4900	17500	43000	105000	
				3.0 V	1050	2100	7250	18000	44500	2600	5300	18000	44500	110000	
				3.3 V	1100	2200	7450	18000	45500	2800	5550	18500	45500	115000	
				3.6 V	1200	2350	7700	18500	46500	3050	5850	19000	47000	115000	
		RTC clocked by LSE quartz in low-drive mode	EN_ULP = 0, LPCAL = 0	1.8 V	710	2050	8650	22000	54000	1750	5150	21500	54500	135000	
				2.4 V	780	2300	9100	23000	57000	1950	5750	23000	57500	140000	
				3.0 V	850	2600	9750	24500	61500	2100	6550	24500	61000	155000	
				3.3 V	1150	2800	10000	25500	64000	2850	7000	25000	63500	160000	
				3.6 V	1250	3000	10500	26500	66500	3150	7450	26000	66000	165000	
			EN_ULP = 0, LPCAL = 1	1.8 V	695	1850	7800	19500	48000	1750	4700	19500	48500	120000	
				2.4 V	750	1950	8000	19500	49000	1850	4850	20000	49500	120000	
				3.0 V	770	2050	8300	20500	50500	1900	5050	20500	51000	125000	
				3.3 V	830	2100	8500	20500	51500	2050	5200	21000	52000	130000	

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 2)}$	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSE quartz in low-drive mode	EN_ULP = 0, LPCAL = 1	3.6 V	870	2150	8750	21000	53000	2200	5400	22000	53000	130000	nA
			EN_ULP = 1, LPCAL = 1	1.8 V	630	1900	8500	21500	53000	1550	4800	21000	53500	130000	
				2.4 V	680	2100	8900	22500	56000	1700	5200	22000	56000	140000	
				3.0 V	740	2300	9400	23500	59500	1850	5750	23500	59000	150000	
				3.3 V	805	2450	9750	24500	61500	2000	6100	24500	61000	155000	
				3.6 V	860	2600	10000	25500	64000	2150	6500	25000	63500	160000	

Table 40. Current consumption in Standby mode

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Standby)}$	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog	EN_ULP = 1	1.8 V	32.5	225	1900	4350	11000	81	560	4700	11000	27500	nA
				2.4 V	50.5	305	1950	5100	13000	125	760	4900	12500	32500	
				3.0 V	70.5	410	2550	5850	15000	175	1000	6300	14500	37500	
				3.3 V	83.0	470	2800	6250	16000	210	1150	7050	15500	40000	
				3.6 V	110	545	3050	6750	17000	275	1350	7700	17000	43000	
			EN_ULP = 0	1.8 V	97.5	245	1200	3700	10500	245	620	3050	9250	26000	
				2.4 V	110	280	1350	4150	12000	275	705	3450	10500	30500	
				3.0 V	125	320	1550	4750	14000	310	805	3900	12000	35000	
				3.3 V	135	350	1700	5100	15000	335	875	4250	12500	37500	
				3.6 V	150	395	1850	5500	16000	375	985	4600	13500	40000	
		Independent watchdog	EN_ULP = 0	1.8 V	190	340	1250	3550	10500	480	850	3100	8850	25000	
				2.4 V	215	385	1450	4000	11500	535	960	3600	10000	29000	
				3.0 V	240	430	1600	4550	13000	600	1100	4050	11500	33000	
				3.3 V	255	470	1750	4850	14000	640	1150	4350	12000	35000	
				3.6 V	280	515	1900	5250	15000	700	1300	4700	13000	37500	
$I_{DD\ (Standby\ with\ RTC)}$	-	RTC clocked by LSI, no independent watchdog	EN_ULP = 0	1.8 V	190	340	1250	3500	10500	480	845	3100	8800	25500	
				2.4 V	215	380	1400	4000	11500	535	955	3550	10000	29000	
				3.0 V	240	435	1600	4550	13000	600	1100	4050	11500	32500	
				3.3 V	255	470	1750	4850	14000	640	1150	4350	12000	35000	
				3.6 V	280	515	1900	5300	15000	705	1300	4700	13000	37500	

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Standby\ with\ RTC)}$	-	RTC clocked by LSI, independent watchdog	EN_ULP = 0	1.8 V	195	340	1250	3500	10000	485	855	3100	8800	25500	nA
				2.4 V	215	385	1400	4000	11500	545	965	3550	10000	29000	
				3.0 V	245	440	1600	4550	13000	615	1100	4050	11500	32500	
				3.3 V	260	475	1750	4850	14000	655	1200	4350	12000	35000	
				3.6 V	285	525	1900	5300	15000	715	1300	4700	13000	37500	
		RTC clocked by LSE, bypassed at 32768 Hz		1.8 V	150	295	1200	3550	10500	370	740	3000	8850	25500	
				2.4 V	195	360	1400	4050	11500	485	905	3500	10000	29000	
				3.0 V	240	435	1650	4650	13500	605	1100	4100	11500	33500	
				3.3 V	270	485	1800	5000	14000	680	1200	4450	12500	35500	
				3.6 V	315	550	1950	5400	15000	785	1400	4900	13500	38000	
		RTC clocked by LSE quartz in low-drive mode	EN_ULP = 0, LPCAL = 0	1.8 V	445	570	1750	4950	14000	1100	1450	4350	12500	35500	
				2.4 V	495	700	2050	5750	16500	1250	1750	5100	14500	41500	
				3.0 V	580	855	2350	6650	19000	1450	2150	5950	16500	48000	
				3.3 V	690	950	2550	7200	20500	1700	2350	6450	18000	52000	
				3.6 V	775	1050	2800	7950	22500	1950	2650	7050	20000	56000	
			EN_ULP = 0, LPCAL = 1	1.8 V	220	410	1600	4650	13500	550	1050	3950	11500	33500	
				2.4 V	260	475	1800	5200	15000	650	1200	4500	13000	37500	
				3.0 V	290	550	2050	5850	16500	730	1350	5150	14500	42000	
				3.3 V	350	595	2200	6250	17500	870	1500	5550	15500	44000	
				3.6 V	385	665	2400	6700	19000	960	1650	6050	16500	47000	
			EN_ULP = 1, LPCAL = 1	1.8 V	160	390	2250	6400	18500	400	980	5650	16000	46000	
				2.4 V	210	505	2650	7500	21500	525	1250	6650	19000	54000	
				3.0 V	240	650	3100	8700	25000	605	1600	7800	21500	63000	
				3.3 V	300	735	3350	9350	27000	745	1850	8400	23500	67500	
				3.6 V	340	840	3650	10000	29000	855	2100	9150	25500	73000	
$I_{DD\ (SRAM2)}$	Supply current to be added in Standby mode when SRAM2 is retained		-	1.8 V	89.0	135	400	9250	23000	175	3350	9500	23000	53000	
				2.4 V	90.0	135	400	9250	22000	180	3350	10000	23000	53500	
				3.0 V	90.0	135	410	9300	21500	180	3400	10000	23500	54000	
				3.3 V	90.0	135	410	9350	21500	180	3400	10000	23500	54500	
				3.6 V	90.5	135	415	9350	22500	185	3450	10500	24000	56500	

Table 41. Current consumption in Shutdown mode

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Shutdown)}$	Supply current in Shutdown mode (backup registers retained), RTC disabled	-	EN_ULP = 0	1.8 V	16.0	91.5	640	2200	6750	40	230	1600	5450	17000	nA
				2.4 V	42.5	140	765	2550	8250	105	345	1900	6350	20500	
				3.0 V	50.0	165	900	2900	9500	125	410	2250	7300	23500	
				3.3 V	52.0	175	975	3150	10000	130	445	2450	7850	25500	
				3.6 V	64.0	210	1100	3450	11000	160	525	2750	8600	27500	
$I_{DD\ (Shutdown\ with\ RTC)}$	Supply current in Shutdown mode (backup registers retained), RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	-	1.8 V	64.0	145	665	2100	6950	160	365	1650	5250	17500	
				2.4 V	120	215	830	2500	7950	300	535	2050	6250	20000	
				3.0 V	165	280	990	2900	9050	415	700	2450	7200	22500	
				3.3 V	190	310	1100	3150	9800	475	780	2750	7850	24500	
				3.6 V	225	370	1250	3450	10500	565	930	3100	8650	26500	
		RTC clocked by LSE quartz	EN_ULP = 0, LPCAL = 0	1.8 V	335	415	1050	3750	11500	840	1050	2750	9350	29000	
				2.4 V	340	540	1300	4400	14500	850	1350	3300	11000	35500	
				3.0 V	400	680	1600	5150	17000	1000	1700	3950	13000	42000	
				3.3V	605	760	1750	5650	18500	1500	1900	4400	14000	46000	
				3.6 V	685	865	1950	6150	19500	1700	2150	4900	15500	49500	
			EN_ULP = 0, LPCAL = 1	1.8 V	195	250	930	2950	9750	490	630	2350	7400	24500	
				2.4 V	215	320	1050	3300	10500	540	800	2750	8300	26500	
				3.0 V	215	375	1100	3750	11500	590	945	3200	9350	29500	
				3.3 V	235	410	1400	4000	12500	665	1050	3500	10000	31000	
				3.6 V	295	470	1550	4350	13000	745	1150	3900	11000	33000	

Table 42. Current consumption in VBAT mode

Symbol	Parameter	Conditions			TYP					MAX					Unit
		-	-	VBAT	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (VBAT)}$	Supply current in VBAT mode, Peripheral current consumption	RTC disabled	-	1.8 V	5.5	8.00	24.5	590	1850	14.5	24.0	62.0	1450	4650	nA
				2.4 V	7.5	9.00	36.5	690	2150	19.0	24.5	91.0	1700	5350	
				3.0 V	9.5	11.5	44.0	795	2450	24.5	30.0	110	2000	6150	
				3.3 V	10	12.0	47.0	860	2650	25.5	30.0	120	2150	6600	
				3.6 V	12.5	14.5	56.5	950	2900	31.0	36.5	140	2350	7200	
		RTC clocked by LSE, bypassed at 32768 Hz	-	1.8 V	50	54.5	79.0	660	1950	125	135	200	1650	4900	

Symbol	Parameter	Conditions			TYP					MAX					Unit
		-	-	VBAT	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (VBAT)}$	Supply current in VBAT mode, Peripheral current consumption	RTC clocked by LSE, bypassed at 32768 Hz	-	2.4 V	67.5	88.0	115	790	2250	170	220	295	2000	5700	nA
				3.0 V	75.5	125	160	950	2650	190	310	400	2350	6600	
				3.3 V	93.5	145	185	1050	2900	235	360	465	2600	7200	
				3.6 V	120	170	220	1200	3200	300	425	555	2950	7950	
		RTC clocked by LSE quartz in low-drive mode	LPCAL = 0	1.8 V	110	265	340	785	2100	270	295	460	1950	5200	
				2.4 V	125	360	435	1100	2400	300	330	525	2800	5950	
				3.0 V	180	475	555	1350	2700	440	505	610	3350	6800	
				3.3 V	195	570	620	1450	2950	490	550	670	3650	7300	
				3.6 V	230	635	695	1600	3150	560	610	740	4000	7950	
			LPCAL = 1	1.8 V	110	120	185	785	2100	275	670	855	1950	5250	
				2.4 V	120	130	210	1100	2350	315	905	1100	2800	5950	
				3.0 V	175	200	245	1350	2700	450	1200	1400	3350	6800	
				3.3 V	195	220	265	1450	2900	490	1400	1550	3650	7350	
				3.6 V	225	245	295	1600	3150	575	1600	1750	4000	7950	

6.3.5.1 *I/O system current consumption*

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull resistors generate a current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in Table 62. I/O static characteristics.

For the output pins, any internal or external pull-up or pull-down resistor and external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see Table 43. Peripheral current consumption), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the internal or external capacitive load connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

6.3.5.2 *On-chip peripheral current consumption*

The current consumption of the on-chip peripherals is given in Table 43. Peripheral current consumption. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in Table 18. Voltage characteristics
- The power consumption of the digital part of the on-chip peripherals is given in Table 43. Peripheral current consumption. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 43. **Peripheral current consumption**

Peripheral		Range 1	Range2	Unit
AHB	BUS matrix[(1)]	0.4	0.4	µA/MHz
	ADC	1.9	0.4	
	CRC	0.7	0.2	
	DMA1	5.3	1.5	
	FLASH	7.9	2.2	
	GPIOA[(2)]	0.2	0.1	
	GPIOB[(2)]	0.3	0.1	
	GPIOC[(2)]	0.2	0.1	
	GPIOD[(2)]	0.3	0.1	
	GPIOF[(2)]	0.1	0.1	
	RNG	1.3	NA	
	TSC	3	0.8	
	ALL AHB bridges	8.7	5.3	
APB	AHB to APB bridge[(3)]	32.7	19.9	
	RTCA	4.4	1.2	
	I2C1[(4)]	0.9	0.3	
	I2C1[(5)]	1.1	0	
	I2C2	1	0.3	
	I2C3[(4)]	0.7	0.2	
	I2C3[(5)]	0.8	0	
	USART1[(4)]	3.1	0	
	USART1[(5)]	0	0	
	USART2[(4)]	3	0.8	
	USART2[(5)]	0	0	
	USART3[(4)]	2.7	0.7	
	USART3[(5)]	0	0	
	LPUART1[(4)]	1.7	0.6	
	LPUART1[(5)]	1.8	0	
	LPUART2[(4)]	1.8	0.6	
	LPUART2[(5)]	1.9	0	
	LPTIM1[(4)]	2	0.6	
	LPTIM1	2.2	0	
	LPTIM2[(4)]	1.5	0.4	
	LPTIM2[(5)]	1.7	0	
	OPAMP	0.2	0.1	
	DAC	1.1	0.3	
	PWR	0.6	0.2	
	SPI2	1.8	0.5	
	SPI3	1.8	0.5	

Peripheral		Range 1	Range2	Unit
APB	TIM1	0.7	0.2	µA/MHz
	TIM2	5.6	1.6	
	TIM6	1	0.3	
	TIM7	1	0.3	
	TIM15	0.6	0.2	
	TIM16	2.9	0	
	WWDG	0.5	0.1	
	SPI1	2.1	0.6	
	SYSCFG	0.3	0.1	
	ALL APB bridges	49	13.6	

1. *The BusMatrix is automatically active when at least one master is ON (CPU, DMA).*
2. *The GPIOx (x= A…F) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).*
3. *The AHB to APB bridge is automatically active when at least one peripheral is ON on the APB.*
4. *Independent clock domain.*
5. *Clock domain.*

6.3.6 Wake-up time from low-power modes and voltage scaling transition times

The wake-up times given in Table 44 are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait for event) instruction.

Table 44. Low-power mode wake-up timings

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wake-up time from Low-power sleep mode to Low-power run mode	Wake-up in flash with flash in power-down during low-power sleep mode (SLEEP_PD = 1 in FLASH_ACR) and with clock MSI = 2 MHz		6	8.3	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in flash	Range 1 or range 2	Wake-up clock MSI = 24 MHz	6.3	6.7	µs
			Wake-up clock HSI16 = 16 MHz	6.5	6.7	
			Wake-up clock MSI = 1 MHz	33.0	36.0	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1 or range 2	Wake-up clock MSI = 24 MHz	1.92	2.30	
			Wake-up clock HSI16 = 16 MHz	1.90	2.00	
			Wake-up clock MSI = 1 MHz	19.0	22.0	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in flash	Range 1 or range 2	Wake-up clock MSI = 24 MHz	11.5	17.5	µs
			Wake-up clock HSI16 = 16 MHz	11.0	13.5	
			Wake-up clock MSI = 1 MHz	35.0	38.4	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1 or range 2	Wake-up clock MSI = 24 MHz	7.2	13.0	

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1 or range 2	Wake-up clock HSI16 = 16 MHz	6.9	8.8	µs
			Wake-up clock MSI = 1 MHz	21.9	25.0	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in flash	Range 1 or range 2	Wake-up clock MSI = 24 MHz	12.0	16.5	µs
			Wake-up clock HSI16 = 16 MHz	13.4	17.0	
			Wake-up clock MSI = 1 MHz	40.0	43.5	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1 or range 2	Wake-up clock MSI = 24 MHz	7.67	12.0	
			Wake-up clock HSI16 = 16 MHz	11.0	17.0	
			Wake-up clock MSI = 1 MHz	26.0	29.0	
t_{WUSTBY}	Wake-up time from Standby mode to Run mode	Range 1	Wake-up clock MSI = 4 MHz	62.0	67.0	µs
			Wake-up clock MSI = 1 MHz	63.0	67.0	
t_{WUSHDN}	Wake-up time from Shutdown mode to Run mode	Range 1	Wake-up clock MSI = 4 MHz	292	360	µs

Table 45. **Regulator mode transition times**

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wake-up time from Low-power run mode to Run mode(1)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(2)	Code run with MSI 16 MHz	20	40	

1. *Time until REGLPF flag is cleared in PWR_SR2.*
2. *Time until VOSF flag is cleared in PWR_SR2.*

Table 46. **Wake-up time using USART/LPUART**

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wake-up time needed to calculate the maximum USART/LPUART baud rate allowing to wake up up from stop mode when USART/LPUART clock source is HSI	Stop 0 mode	-	1.7	µs
		Stop 1 mode and Stop 2 mode	-	8.5	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in Section 6.3.14: I/O port characteristics. However, the recommended clock input waveform is shown in Figure 15. AC timing diagram for high-speed external clock source .

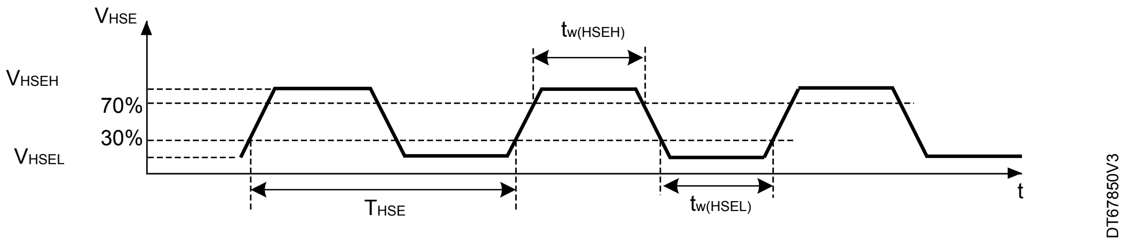
Table 47. **High-speed external user clock characteristics**

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	19	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

Figure 15. AC timing diagram for high-speed external clock source



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

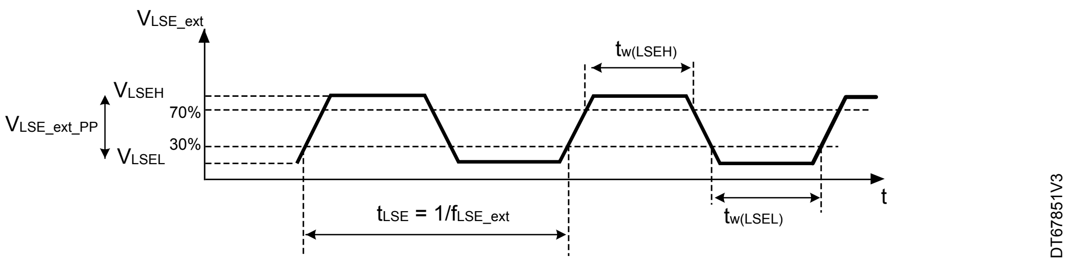
The external clock signal has to respect the I/O characteristics in Section 6.3.14: I/O port characteristics. However, the recommended clock input waveform is shown in Figure 16. AC timing diagram for low-speed external clock source.

Table 48. Low-speed external user clock characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

Figure 16. AC timing diagram for low-speed external clock source



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in Table 49. HSE oscillator characteristics. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 49. HSE oscillator characteristics

Specified by design, not tested in production.

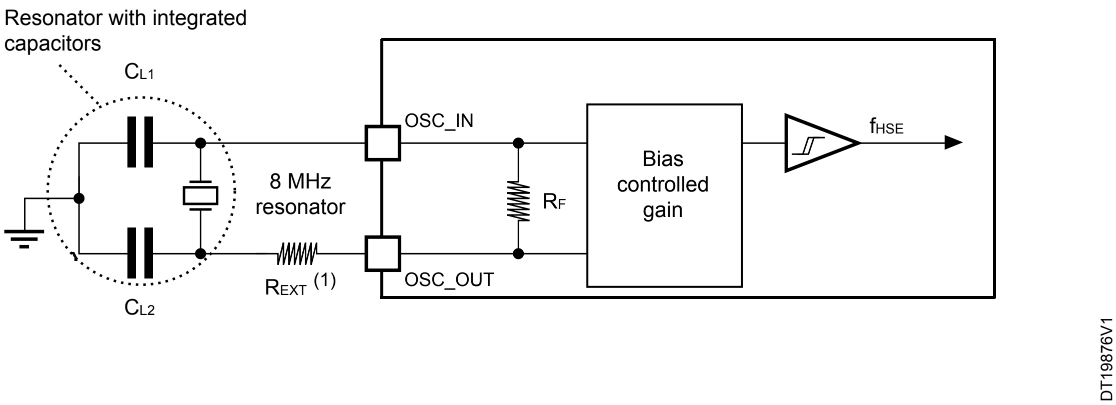
Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup[2]	-	-	5.5	mA
		V_{DD} = 3 V, R_m = 30 Ω, C_L = 10 pF @ 8 MHz	-	0.58	-	
		V_{DD} = 3 V, R_m = 45 Ω, C_L = 10 pF @ 8 MHz	-	0.59	-	
		V_{DD} = 3 V, R_m = 30 Ω, C = 5 pF @ 48 MHz	-	0.89	-	
		V_{DD} = 3 V, R_m = 30 Ω, C_L = 10 pF @ 48 MHz	-	1.14	-	
		V_{DD} = 3 V, R_m = 30 Ω, C_L = 20 pF @ 48 MHz	-	1.94	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$[3]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*
2. *This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time*
3. *$t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer*

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 17. Typical application with an 8 MHz crystal). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 17. **Typical application with an 8 MHz crystal**



1. *R_{EXT} value depends on the crystal characteristics.*

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in Table 50. LSE oscillator characteristics (f_{LSE} = 32.768 kHz). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 50. **LSE oscillator characteristics (f_{LSE} = 32.768 kHz)**

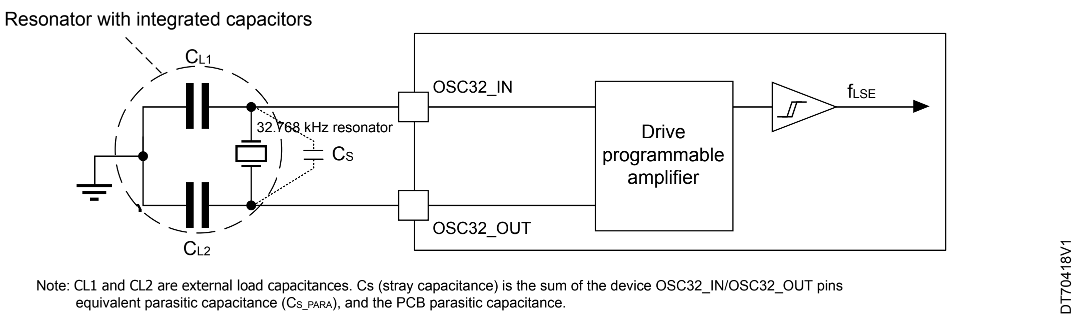
Specified by design, not tested in production.

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00, low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01, medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10, medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11, high drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, high drive capability	-	-	2.7	
$t_{SU(LSE)}$[2]	Startup time	V_{DD} is stabilized	-	2	-	s

1. *Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".*
2. *$t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer*

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. **Typical application with a 32.768 kHz crystal**



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in Table 51. HSI16 oscillator characteristics are derived from tests performed under ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions. The provided curves are evaluated by characterization, not tested in production.

High-speed internal (HSI16) RC oscillator

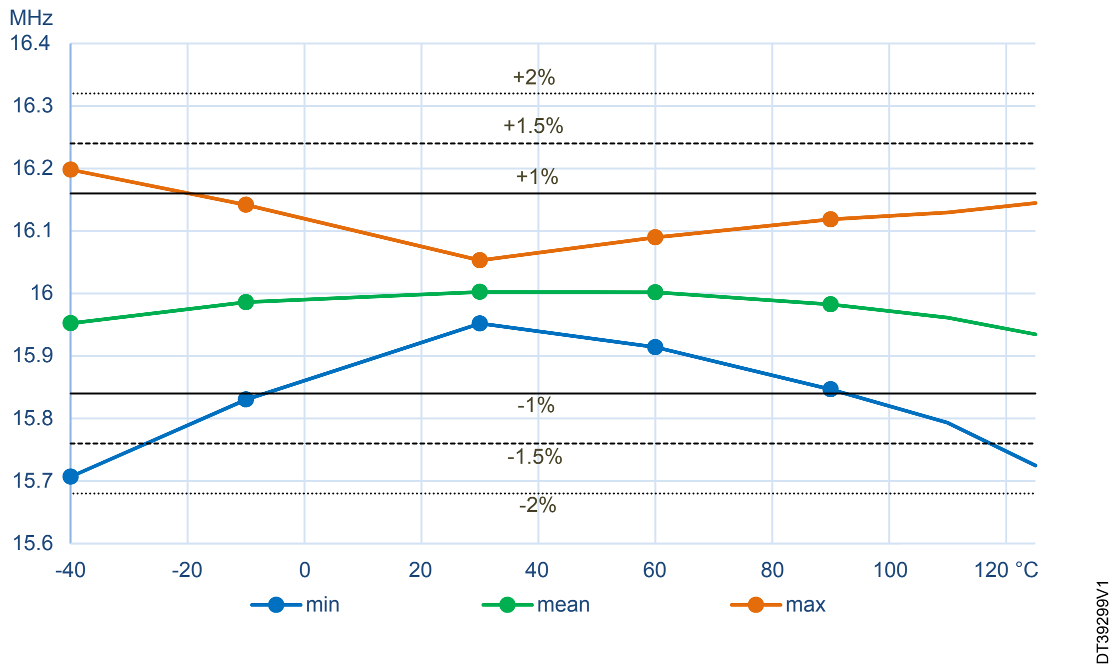
Table 51. **HSI16 oscillator characteristics**

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	From code 127 to 128	-8	-6	-4	%
		From code 63 to 64 From code 191 to 192	-5.8	-3.8	–1.8	
		For all other code increments	0.2	0.3	0.4	
DuCy(HSI16)[(1)]	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)[(1)]	HSI16 oscillator start-up time	-	-	0.8	1.2	μs
t_{stab}(HSI16)[(1)]	HSI16 oscillator stabilization time	-	-	3	5	μs
I_{DD}(HSI16)[(1)]	HSI16 oscillator power consumption	-	-	155	190	μA

1. *Specified by design, not tested in production.*

Figure 19. **HSI16 frequency versus temperature**



Multi-speed internal (MSI) RC oscillator

Table 52. **MSI oscillator characteristics**

Evaluated by characterization, not tested in production.

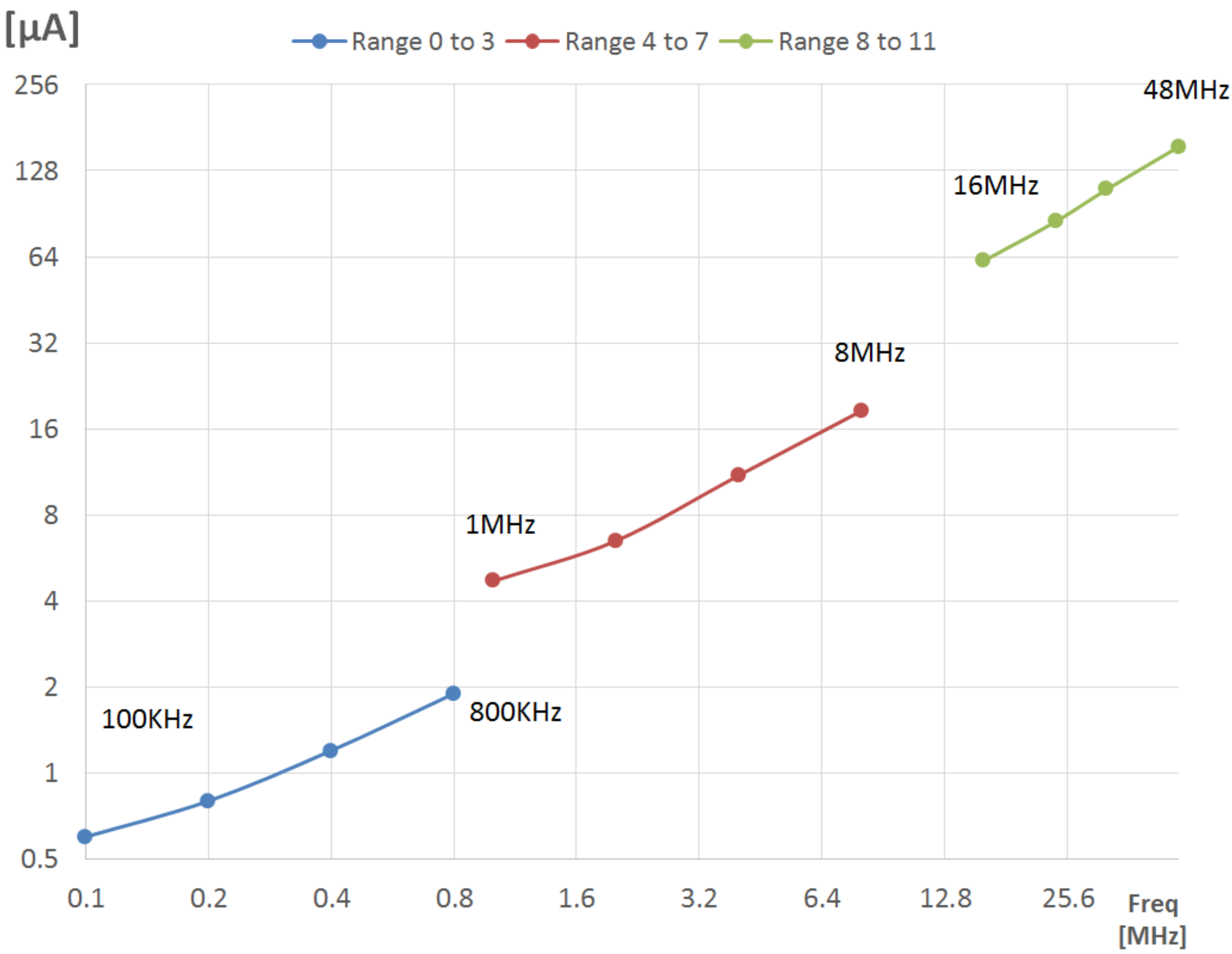
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD} = 3 V and T_A = 30 °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	kHz
			Range 2	394.8	400	405.2	kHz
			Range 3	789.6	800	810.4	kHz
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	MHz
			Range 6	3.948	4	4.052	MHz
			Range 7	7.896	8	8.104	MHz
			Range 8	15.79	16	16.21	MHz
			Range 9	23.69	24	24.31	MHz
			Range 10	31.58	32	32.42	MHz
			Range 11	47.38	48	48.62	MHz
		PLL mode XTAL = 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	kHz
			Range 2	-	393.216	-	kHz
			Range 3	-	786.432	-	kHz
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	MHz

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD} = 3 V and T_A = 30 °C	PLL mode XTAL = 32.768 kHz	Range 6		-	3.998	-	MHz
			Range 7		-	7.995	-	
			Range 8		-	15.991	-	
			Range 9		-	23.986	-	
			Range 10		-	32.014	-	
			Range 11		-	48.005	-	
Δ_{TEMP}(MSI)[1]	MSI oscillator frequency drift over temperature	MSI mode	T_A = 0 to 85 °C		-3.5	-	3	%
			T_A = -40 to 125 °C		-8	-	6	
Δ_{VDD}(MSI)[1]	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD} = 1.62 V to 3.6 V	-1.2	-	0.5	%
				V_{DD} = 2.4 V to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD} = 1.62 V to 3.6 V	-2.5	-	0.7	
				V_{DD} = 2.4 V to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD} = 1.62 V to 3.6 V	-5	-	1.2	
				V_{DD} = 2.4 V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}$ (MSI)[1][3]	Frequency variation in sampling mode[2]	MSI mode	T_A = -40 to 85 °C		-	1	2	%
			T_A = -40 to 125 °C		-	2	4	
CC jitter(MSI)[3]	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)[3]	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
t_{SU}(MSI)[3]	MSI oscillator start-up time	Range 0		-	-	10	20	µs
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
t_{STAB}(MSI)[3]	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	
I_{DD}(MSI)[3]	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{DD}(MSI)(3)	MSI oscillator power consumption	MSI and PLL mode	Range 8	-	-	62	80	μA
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. *This is a deviation for an individual part once the initial frequency has been measured.*
2. *Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.*
3. *Specified by design, not tested in production.*

Figure 20. Typical current consumption versus MSI frequency



Low-speed internal (LSI) RC oscillator

Table 53. LSI oscillator characteristics

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
t_{SU}(LSI)(1)	LSI oscillator start-up time	-	-	80	130	μs
t_{STAB}(LSI)(1)	LSI oscillator stabilization time	5% of final frequency	-	125	180	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}(LSI)[1]	LSI oscillator power consumption	-	-	110	180	nA

1. *Specified by design, not tested in production.*

6.3.9 PLL characteristics

The parameters given in Table 54. PLL characteristics are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Table 54. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock frequency[1]	-	2.66	-	16	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	3.09	-	122	MHz
		Voltage scaling Range 2	3.09	-	40	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	12	-	128	MHz
		Voltage scaling Range 2	12	-	33	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	12	-	64	MHz
		Voltage scaling Range 2	12	-	16	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	MHz
		Voltage scaling Range 2	96	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	μs
Jitter	RMS cycle-to-cycle jitter	System clock 56 MHz	-	50	-	±ps
	RMS period jitter		-	40	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}not found	VCO freq = 96 MHz	-	200	260	μA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. *Make sure to use the appropriate division factor M to obtain the specified PLL input clock values.*

6.3.10 Flash memory characteristics

Table 55. Flash memory characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	85	125	μs
		Burst mode	48	48	
t_{prog_row}	Row (32 double word) programming time	Normal programming	2.7	4.6	ms
		Fast programming	1.7	2.8	
t_{prog_page}	Page (2 Kbytes) programming time	Normal programming	21.8	36.6	
		Fast programming	13.7	22.4	
t_{ERASE}	Page (2 Kbytes) erase time	-	22.0	40.0	
t_{prog_bank}	One 64-Kbyte bank programming time[1]	Normal programming	1.4	2.4	s
		Fast programming	0.9	1.5	
t_{ME}	Mass erase time	-	22.1	40.1	ms

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(Flash\ A)}$	Average consumption from V_{DD}	Programming	3	-	mA
		Page erase	3	-	
		Mass erase	5		
$I_{DD(Flash\ P)}$	Maximum current (peak)	Programming, 2 µs peak duration	7	-	
		Erase, 41 µs peak duration	7	-	

1. *The values provided also apply to devices with less flash memory than one 64-Kbyte bank.*

Table 56. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min[1]	Unit
N_{END}	Endurance	T_A = -40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Years
		1 kcycle[2] at T_A = 105 °C	15	
		1 kcycle[2] at T_A = 125 °C	7	
		10 kcycles[2] at T_A = 55 °C	30	
		10 kcycles[2] at T_A = 85 °C	15	
		10 kcycles[2] at T_A = 105 °C	10	

1. *Evaluated by characterization, not tested in production.*
2. *Cycling performed over the whole temperature range.*

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 57. EMS characteristics. They are based on the EMS levels and classes defined in application note AN1709.

Table 57. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 48 MHz, LPQF64 conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 48 MHz, LPQF64 conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 58. EMI characteristics for f_{HSE} = 8 MHz and f_{HCLK} = 48 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak	V_{DD} = 3.6 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	1	dBµV
			30 MHz to 130 MHz	0	
			130 MHz to 1 GHz	2	
			1 GHz to 2 GHz	8	
	Level		0.1 MHz to 2 GHz	2	-

1. *Refer to AN1709 “EMI radiated test” section.*
2. *Refer to AN1709 “EMI level classification” section.*

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 59. ESD absolute maximum ratings

TBD stands for "to be defined".

Symbol	Ratings	Conditions	Package	Class	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	All	2D	2000	V

Symbol	Ratings	Conditions	Package	Class	Maximum value	Unit
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESDA/ JEDEC-002	WLCSP27	TBD	TBD	V
			All others	C2a	500	

1. *Evaluated by characterization, not tested in production.*

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 60. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +130 °C conforming to JESD78A	II

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the 5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in Table 61. I/O current injection susceptibility.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 61. I/O current injection susceptibility

Evaluated by characterization, not tested in production.

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PA4, PA5	-5	N/A[1]	mA
	Injected current on PA4, PA5 pins	-5	0	

1. *Injection is not possible.*

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 62. I/O static characteristics are derived from tests performed under the conditions summarized in Section 6.3.1: General operating conditions. All I/Os are designed as CMOS- and TTL-compliant.

Note: For information on GPIO configuration, refer to the application note AN4899 "STM32 GPIO configuration for hardware settings and low-pow er consumption" available from the ST website www.st.com.

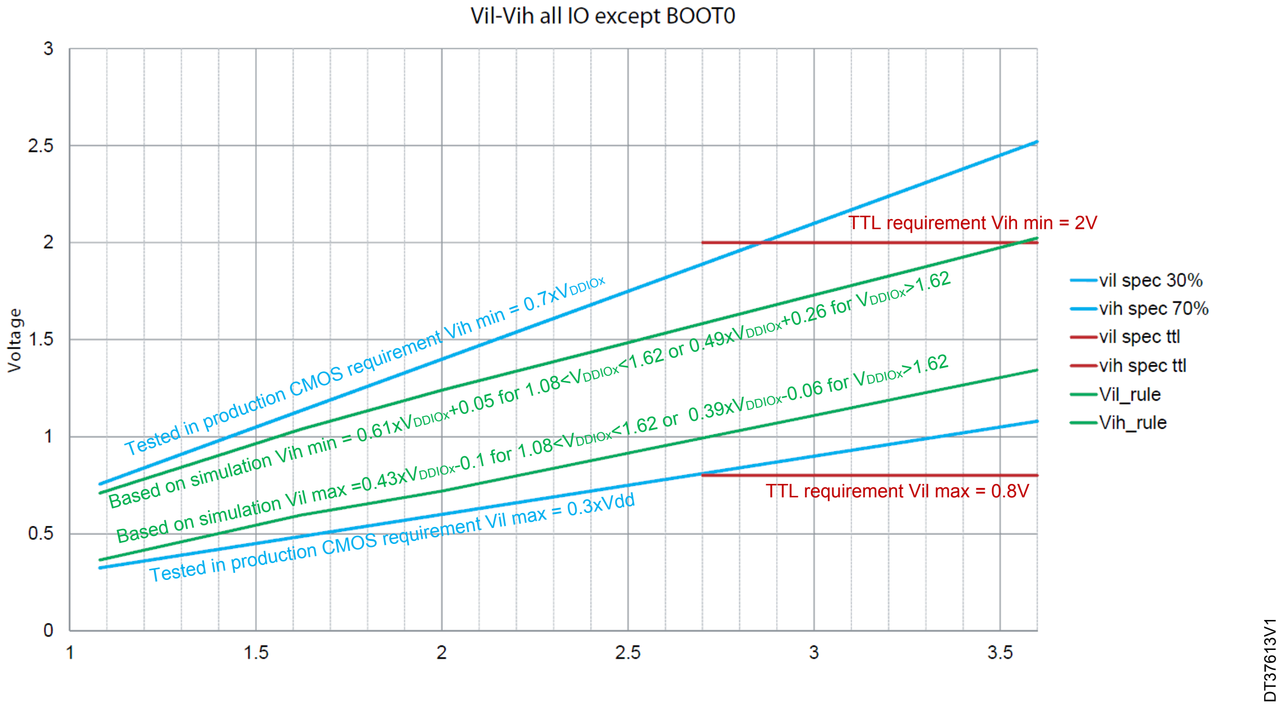
Table 62. **I/O static characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	1.62 V < V_{DDIOx} < 3.6 V	-	-	0.3 x V_{DDIOx} (2)	V
	I/O input low level voltage	1.62 V < V_{DDIOx} < 3.6 V	-	-	0.39 x V_{DDIOx} - 0.06(3)	
V_{IH}(1)	I/O input high level voltage	1.62 V < V_{DDIOx} < 3.6 V	0.7 x V_{DDIOx} (2)	-	-	V
	I/O input high level voltage	1.62 V < V_{DDIOx} < 3.6 V	0.49 x V_{DDIOX} + 0.26 (3)	-	-	
V_{hys}(3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V < V_{DDIOx} < 3.6 V	-	200	-	mV
I_{lkg}(4)	FT_xx input leakage current(3)(5)	V_{IN} ≤ Max(V_{DDXXX})(6)(7)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX}) + 1 V(6)(7)	-	-	650	
		Max(V_{DDXXX}) + 1 V < V_{IN} ≤ 5.5 V(6)(7)	-	-	200	
	PC3 I/O	V_{IN} ≤ Max(V_{DDXXX})(6)(7)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX}) + 1 V(6)(7)	-	-	2500(3)	
		Max(V_{DDXXX}) + 1 V < V_{IN} ≤ 5.5 V(6)(7)	-	-	250	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(6)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6V(6)	-	-	2000(3)	
R_{PU}	Weak pull-up equivalent resistor(8)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(8)	V_{IN} = V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. *Refer to Figure 21. I/O input characteristics.*
2. *Tested in production.*
3. *Specified by design, not tested in production.*
4. *This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula:*
   $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] × I_{lkg}(Max).
5. *All FT_xx GPIOs except FT_u and PC3 I/O.*
6. *Max(V_{DDXXX}) is the maximum value of all the I/O supplies. Refer to Table: Legend/Abbreviations used in the pinout table.*
7. *To sustain a voltage higher than Min(V_{DD}, V_{DDA}) + 0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.*
8. *Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).*

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in Figure 21. I/O input characteristics.

Figure 21. I/O input characteristics



Current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

GPIOs PC13, PC14 and PC15 are supplied through the power switch, limiting source capability up to 3 mA only.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section 6.2: Absolute maximum ratings:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see Table 18. Voltage characteristics).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 18. Voltage characteristics).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions. All I/Os are CMOS- and TTL-compliant (FT or TT unless otherwise specified).

Table 63. Output voltage characteristics

The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 18. Voltage characteristics, , and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port [1] $\|I_{IO}\|$ = 8 mA[2] $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx} - 0.4	-	
V_{OL}[3]	Output low level voltage for an I/O pin	TTL port[1] $\|I_{IO}\|$ = 8 mA[4] $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}[3]	Output high level voltage for an I/O pin		2.4	-	

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (3)	Output low level voltage for an I/O pin	PC13, PC14 and PC15 $\|I_{IO}\|$ = 3 mA V_{DDIOx} ≥ 2.7 V	-	0.07	V
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DDIOx} - 0.35	-	
V_{OL} (3)	Output low level voltage for an I/O pin	$\|I_{IO}$ = 20 mA(4) V_{DDIOx} ≥ 2.7 V	-	1.3	
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DDIOx} - 1.3	-	
V_{OL} (3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA(2) V_{DDIOx} ≥ 1.62 V	-	0.45	
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DDIOx} - 0.45	-	
V_{OLFM+} (3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA V_{DDIOx} ≥ 2.7 V	-	0.4	
		$\|I_{IO}\|$ = 10 mA V_{DDIOx} ≥ 1.62 V	-	0.4	

1. *TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*
2. *PC13, PC14 and PC15 are tested/characterized at their maximum current of 3 mA.*
3. *Specified by design, not tested in production.*
4. *Not applicable to PC13, PC14 and PC15.*

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in Figure 22. I/O AC characteristics definition and Table 64. I/O AC characteristics, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Table 64. I/O AC characteristics

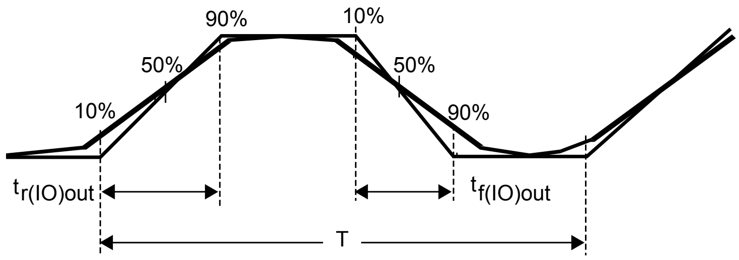
1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0503 reference manual for a description of GPIO Port configuration register.
2. Specified by design, not tested in production.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(1)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(1)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(1)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.62 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(2)		-	5	ns

1. *This value represents the I/O capability but the maximum system frequency is limited to 56 MHz.*
2. *The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.*

Figure 22. I/O AC characteristics definition



Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

DT32132V4

1. *Refer to Table 64. I/O AC characteristics.*

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

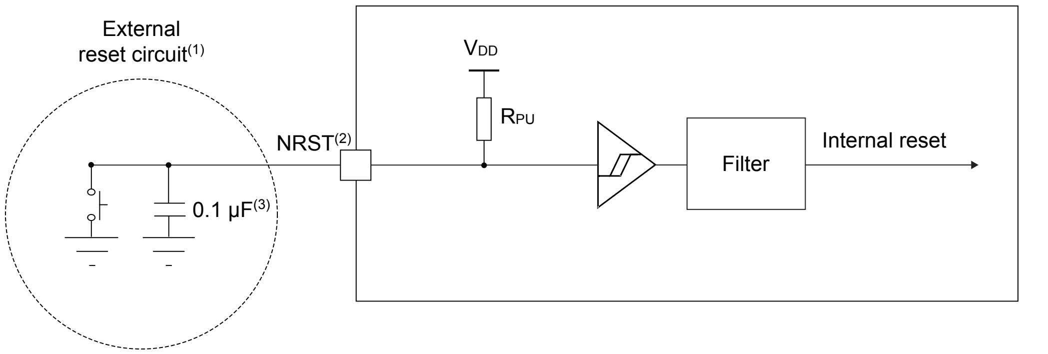
Table 65. NRST pin characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 × V_{DDIOx}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7 × V_{DDIOx}	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor[(1)]	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. *The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).*

Figure 23. Recommended NRST pin protection



1. *The reset network protects the device against parasitic resets.*
2. *The user must ensure that the voltage level on the NRST pin can go above the $V_{IH(NRST)}$ minimum level specified in Table 65. NRST pin characteristics during each power on, otherwise the device does not exit from reset. This is applicable to all NRST configurations selected through the NRST_MODE[1:0] bitfield of the FLASH_OPTR register, including GPIO mode.*
3. *The external capacitor on NRST must be placed as close as possible to the device.*

6.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 66. EXTI Input Characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

6.3.17 Analog switches booster

Table 67. Analog switches booster characteristics

Specified by design, not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs

Symbol	Parameter	Min	Typ	Max	Unit
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

6.3.18 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in Table 68. ADC characteristics are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Note: It is recommended to perform a calibration after each power-up.

Table 68. ADC characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	-	V_{DDA}			
f_{ADC}	ADC clock frequency	Range 1	0.14	-	35	MHz
		Range 2	0.14	-	16	
f_s	Sampling rate	12 bits	-	-	2.50	MSps
		10 bits	-	-	2.92	
		8 bits	-	-	3.50	
		6 bits	-	-	4.38	
f_{TRIG}	External trigger frequency	f_{ADC} = 35 MHz; 12 bits	-	-	2.33	MHz
		12 bits	-	-	$f_{ADC}/15$	
V_{AIN}(2)	Conversion voltage range	-	V_{SSA}	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	ADC power-up time	-	2			Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 35 MHz	2.35			µs
		-	82			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency	CKMODE = 00	2	-	3	$1/f_{ADC}$
		CKMODE = 01	6.5			$1/f_{PCLK}$
		CKMODE = 10	12.5			
		CKMODE = 11	3.5			
ts	Sampling time	f_{ADC} = 35 MHz; V_{DDA} > 2V	0.043	-	4.59	µs
			1.5	-	160.5	$1/f_{ADC}$
		f_{ADC} = 35 MHz; V_{DDA} < 2V	0.1	-	4.59	µs
			3.5	-	160.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 35 MHz Resolution = 12 bits	0.40	-	4.95	µs
		Resolution = 12 bits	t_s + 12.5 cycles for successive approximation = 14 to 173			$1/f_{ADC}$
t_{IDLE}	Laps of time allowed between two conversions without rearm	-	-	-	100	µs
$I_{DDA(ADC)}$	ADC consumption from V_{DDA}	f_s = 2.5 MSps	-	410	-	µA
		f_s = 1 MSps	-	164	-	
		f_s = 10 kSps	-	17	-	
$I_{DDV(ADC)}$	ADC consumption from V_{REF+}	f_s = 2.5 MSps	-	65	-	µA
		f_s = 1 MSps	-	26	-	
		f_s = 10 kSps	-	0.26	-	

1. *I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when V_{DDA} ≥ 2.4 V.*
2. *V_{REF+} is internally connected to V_{DDA}. Refer to Section 4: Pinouts/ballouts, pin description, and alternate functions for further details.*

Table 69. Maximum ADC R_{AIN}

Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN} (1)(2) (Ω)
12 bits	1.5(3)	43	50
	3.5	100	680
	7.5	214	2200
	12.5	357	4700
	19.5	557	8200
	39.5	1129	15000
	79.5	2271	33000
	160.5	4586	50000
10 bits	1.5(3)	43	68
	3.5	100	820
	7.5	214	3300
	12.5	357	5600
	19.5	557	10000
	39.5	1129	22000
	79.5	2271	39000
	160.5	4586	50000
8 bits	1.5(3)	43	82
	3.5	100	1500
	7.5	214	3900
	12.5	357	6800
	19.5	557	12000
	39.5	1129	27000

Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN} [(1)(2)] (Ω)
8 bits	79.5	2271	50000
	160.5	4586	50000
6 bits	1.5[(3)]	43	390
	3.5	100	2200
	7.5	214	5600
	12.5	357	10000
	19.5	557	15000
	39.5	1129	33000
	79.5	2271	50000
	160.5	4586	50000

1. *I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when $V_{DDA} \geq$ 2.4 V.*
2. *Specified by design, not tested in production.*
3. *Only allowed with V_{DDA} > 2 V*

Table 70. ADC accuracy

1. Evaluated by characterization, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. Injecting negative current on any analog input pin significantly reduces the accuracy of A-to-D conversion of signal on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins susceptible to receive negative current.

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
ET	Total unadjusted error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	3	6	LSB
		2 V < $V_{DDA}=V_{REF+}$ < 3.6 V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; T_A = entire range	-	3	6.5	
		1.65 V < $V_{DDA}=V_{REF+}$ < 3.6 V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \le 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \le 1.1$ MSps;	-	3	7.5	
EO	Offset error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	1.5	5	LSB
		2 V < $V_{DDA} = V_{REF+}$ < 3.6 V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; T_A = entire range	-	1.5	5.5	
		1.65 V < $V_{DDA}=V_{REF+}$ < 3.6 V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \le 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \le 1.1$ MSps;	-	1.5	6	
EG	Gain error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	3	3.5	LSB
		2 V < $V_{DDA} = V_{REF+}$ < 3.6 V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; T_A = entire range	-	3	5	
		1.65 V < $V_{DDA} = V_{REF+}$ < 3.6 V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \le 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \le 1.1$ MSps;	-	3	6.5	
ED	Differential linearity error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	1.2	2.5	LSB
		2 V < $V_{DDA} = V_{REF+}$ < 3.6 V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; T_A = entire range	-	1.2	2.5	
		1.65 V < $V_{DDA} = V_{REF+}$ < 3.6 V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \le 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \le 1.1$ MSps;	-	1.2	2.5	
EL	Integral linearity error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	2.5	3	LSB

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
EL	Integral linearity error	2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	2.5	3.5	LSB
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	-	2.5	3.5	
ENOB	Effective number of bits	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	10.1	10.2	-	bit
		2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	9.6	10.2	-	
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	9.5	10.2	-	
SINAD	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	62.5	63	-	dB
		2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	59.5	63	-	
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	59	63	-	
SNR	Signal-to-noise ratio	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	63	64	-	dB
		2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	60	64	-	
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	60	64	-	
THD	Total harmonic distortion	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	-	-74	-73	dB
		2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	-74	-70	
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	-	-74	-70	

1. *I/O analog switch voltage booster enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when V_{DDA} ≥ 2.4 V.*

Figure 24. **ADC accuracy characteristics**

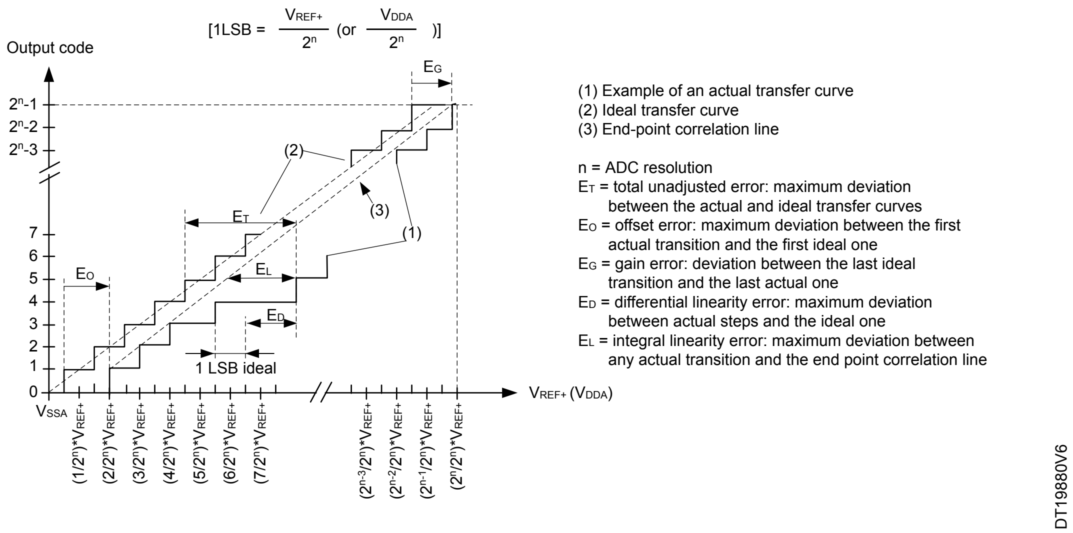
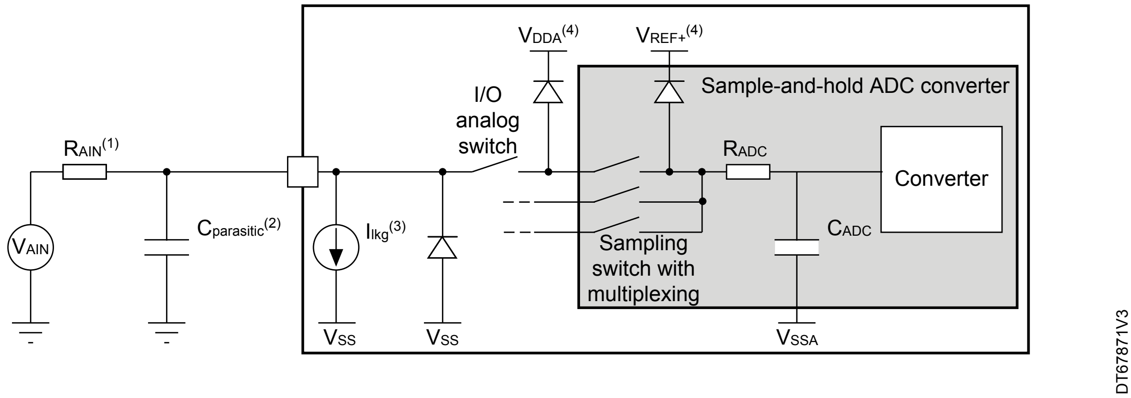


Figure 25. **Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function**



1. *Refer to Table 68. ADC characteristics for the values of R_{AIN} and C_{ADC}.*
2. *$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Table 62. I/O static characteristics for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.*
3. *Refer to Table 62. I/O static characteristics for the values of I_{lkg}.*
4. *Refer to Section 3.6.1: Power supply schemes.*

6.3.18.1 *General PCB design guidelines*

Power supply decoupling should be performed as shown in Figure 12. Power supply scheme. The 100 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.19 Temperature sensor characteristics

Table 71. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope[2]	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)[3]	0.742	0.76	0.785	V
$t_{START(TS\_BUF)}$[1]	Sensor Buffer Start-up time in continuous mode[4]	-	8	15	µs
t_{START}[1]	Start-up time when entering in continuous mode[4]	-	70	120	µs
t_{S_temp}[1]	ADC sampling time when reading the temperature	5	-	-	µs
$I_{DD(TS)}$[1]	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. *Specified by design, not tested in production.*
2. *Evaluated by characterization, not tested in production.*
3. *Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.*
4. *Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.*

6.3.20 V_{BAT} monitoring characteristics

Table 72. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	3×39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er[1]	Error on Q	-10	-	10	%
t_{S_vbat}[1]	ADC sampling time when reading the VBAT	12	-	-	µs

1. *Specified by design, not tested in production.*

Table 73. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.21 Digital-to-analog converter characteristics

Table 74. DAC characteristics

Specified by design, not tested in production.

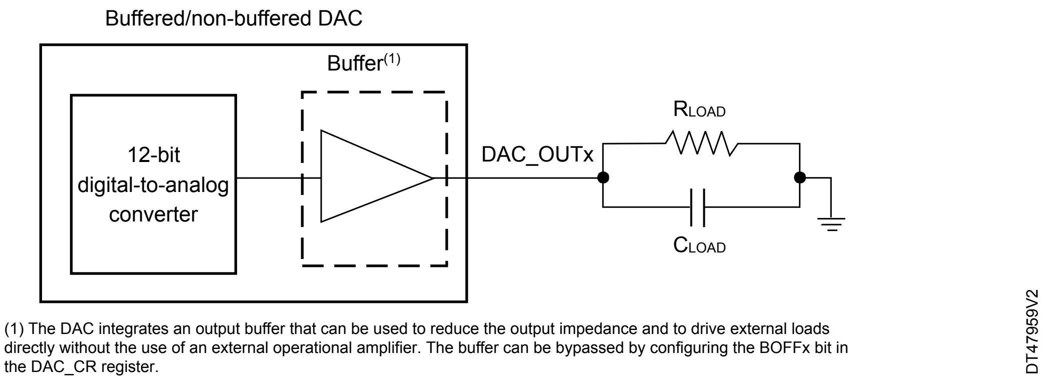
<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="2">V_{DDA}</td><td rowspan="2">Analog supply voltage for DAC ON</td><td colspan="2">DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)</td><td>1.71</td><td>-</td><td rowspan="2">3.6</td><td rowspan="2">V</td></tr>
<tr><td colspan="2">Other modes</td><td>1.80</td><td>-</td></tr>
<tr><td>V_{REF+}</td><td>Positive reference voltage</td><td colspan="2">-</td><td colspan="3">V_{DDA}</td><td>V</td></tr>
<tr><td rowspan="2">R_L</td><td rowspan="2">Resistive load</td><td rowspan="2">DAC output buffer ON</td><td>connected to V_{SSA}</td><td>5</td><td>-</td><td>-</td><td rowspan="2">kΩ</td></tr>
<tr><td>connected to V_{DDA}</td><td>25</td><td>-</td><td>-</td></tr>
</table>

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} - 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}[1]	Wake-up time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB
$T_{W\_to\_W}$	Minimum time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB)	DAC_MCR:MODEx[2:0] = 000 or 001 CL ≤ 50 pF; RL ≥ 5 kΩ		1	-	-	µs
		DAC_MCR:MODEx[2:0] = 010 or 011 CL ≤ 10 pF		1.4	-	-	
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-[2]	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
$I_{DDA(DAC)}$	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDA(DAC)}$	DAC consumption from V_{DDA}	Sample and hold mode, C_{SH} = 100 nF		-	315 x T_{on}/(T_{on}+T_{off})(3)	670 x T_{on}/(T_{on}+T_{off})(3)	µA
$I_{DDV(DAC)}$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x T_{on}/(T_{on}+T_{off})(3)	400 x T_{on}/(T_{on}+T_{off})(3)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x T_{on}/(T_{on}+T_{off})(3)	205 x T_{on}/(T_{on}+T_{off})(3)	

1. *In buffered mode, the output can overshoot above the final value for low input code (starting from min value).*
2. *Refer to Table 62. I/O static characteristics.*
3. *T_{on} is the Refresh phase duration. T_{off} is the Hold phase duration. Refer to RM0503 reference manual for more details.*

Figure 26. 12-bit buffered / non-buffered DAC



1. *The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.*

.

Table 75. DAC accuracy

Specified by design, not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity(1)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(2)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(2)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Offset	Offset error at code 0x800[2]	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 1.8 V	-	-	±25	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001[3]	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error[4]	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	11.5	-	

1. *Difference between two consecutive codes - 1 LSB.*
2. *Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.*
3. *Difference between the value measured at Code (0x001) and the ideal value.*
4. *Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2) V when buffer is ON.*

6.3.22 Comparator characteristics

Table 76. COMP characteristics

Specified by design, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG} [(1)]	Scaler input voltage	-		V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D [(2)]	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		4	8	16	
		Medium hysteresis		8	15	30	
		High hysteresis		15	27	52	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	
I_{bias}	Comparator input bias current	-		-	-	-[(3)]	nA

1. *Refer to Table 24. Embedded internal voltage reference.*
2. *Evaluated by characterization, not tested in production.*
3. *Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in Table 62. I/O static characteristics.*

6.3.23 Operational amplifiers characteristics

Table 77. OPAMP characteristics

Evaluated by characterization, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage[1]	-		1.8	-	3.6	V
CMIR	Common mode input range	-		0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	25 °C, No Load on output.		-	-	±1.5	mV
		All voltage/temperature		-	-	±3	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode		-	±5	-	µV/°C
		Low-power mode		-	±10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-		-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-		-	1	1.35	
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR[2]	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AO	Open loop gain	Low-power mode		45	110	-	dB
V_{OHSAT}[2]	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} -100	-	-	mV
		Low-power mode		V_{DDA} -50	-	-	
V_{OLSAT}[2]	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	-	5	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input		-	-	-[3]	nA
PGA gain[2]	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	
$R_{network}$	R2/R1 internal resistance values in PGA mode[4]	PGA Gain = 2		-	80/80	-	kΩ/kΩ
		PGA Gain = 4		-	120/ 40	-	
		PGA Gain = 8		-	140/ 20	-	
		PGA Gain = 16		-	150/ 10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/2	-	MHz
		Gain = 4	-	-	GBW/4	-	
		Gain = 8	-	-	GBW/8	-	
		Gain = 16	-	-	GBW/16	-	
en	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	-	500	-	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	-	600	-	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	-	180	-	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	-	290	-	
I_{DDA}(OPAMP)[2]	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode	-	120	260	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}(OPAMP)(2)	OPAMP consumption from V_{DDA}	Low-power mode	no Load, quiescent mode	-	45	100	µA

1. *The temperature range is limited to 0 °C-125 °C when V_{DDA} is below 2 V*
2. *Evaluated by characterization, not tested in production.*
3. *Mostly I/O leakage, when used in analog mode. Refer to I_{lkg} parameter in Table 62. I/O static characteristics.*
4. *R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1*

6.3.24 Timer characteristics

The parameters given in the following tables are specified by design, and not tested in production.

Refer to Section 6.3.14: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 78. TIMx characteristics

TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.8	-	ns
fEXT	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
ResTIM	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1363.1	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.34	s

Table 79. IWDG min/max timeout period at 32 kHz (LSI)

The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

Table 80. WWDG min/max timeout at 56 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0358	2.2938	ms
2	1	0.0717	4.5875	
4	2	0.1434	9.1750	

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
8	3	0.2867	18.3501	ms

6.3.25 I^{2}C-bus interface characteristics

The I2C interface meets the timings requirements of the I^{2}C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

When the I2C peripheral is properly configured, the I2C timings requirements are specified by design, and not tested in production (refer to RM0503 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to Section 6.3.14: I/O port characteristics for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 81. I2C analog filter characteristics

Specified by design, not tested in production.

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(1)	205(2)	ns

1. *Spikes with widths below $t_{AF(min)}$ are filtered.*
2. *Spikes with widths above $t_{AF(max)}$ are not filtered*

6.3.26 USART characteristics

Unless otherwise specified, the parameters given in Table 82 are derived from tests performed under the ambient temperature, f_{PCLK} frequency and supply voltage conditions summarized in Section 6.3.1: General operating conditions. The additional general conditions are:

- Output speed is set to OSPEEDRy[1:0] = 11 (output speed)
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5×V_{DD}
- Voltage scale is set to VOS[1:0] = 01

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternatefunction characteristics (NSS, CK, TX, and RX for USART).

Table 82. USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	6.75	MHz
		Slave mode	-	-	18	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker} + 2	-	-	nsnsns
$t_{h(NSS)}$	NSS hold time		0.5	-	-	
$t_{w(CKH)}$	SCK high time	Master mode	1 / f_{CK} / 2 - 1	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1	
$t_{w(CKL)}$	SCK low time					
$t_{su(RX)}$	Data input setup time	Master mode	22	-	-	
		Slave mode	5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	
		Slave mode	0.5	-	-	
$t_{v(TX)}$	Data output valid time,	Master mode	0	0.5	1	
		Slave mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	16	-	19.5	
		Slave mode, 1.71 V ≤ V_{DD} ≤ 3.6 V	16	-	27.5	
$t_{h(TX)}$	Data output hold time	Master mode	0	-	-	
		Master mode	10	-	-	

Figure 27. USART timing diagram in SPI master mode

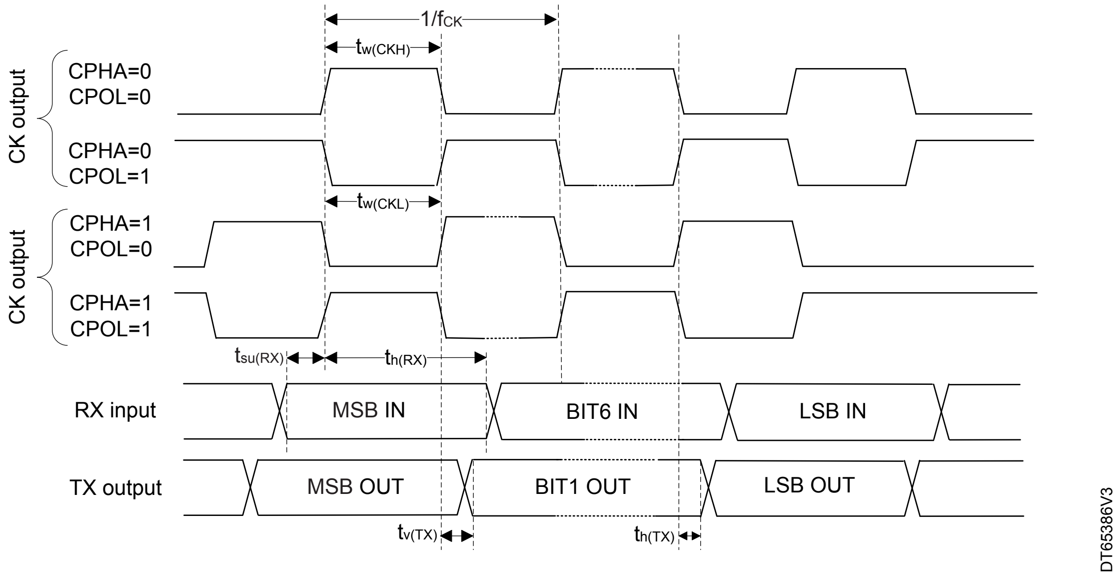
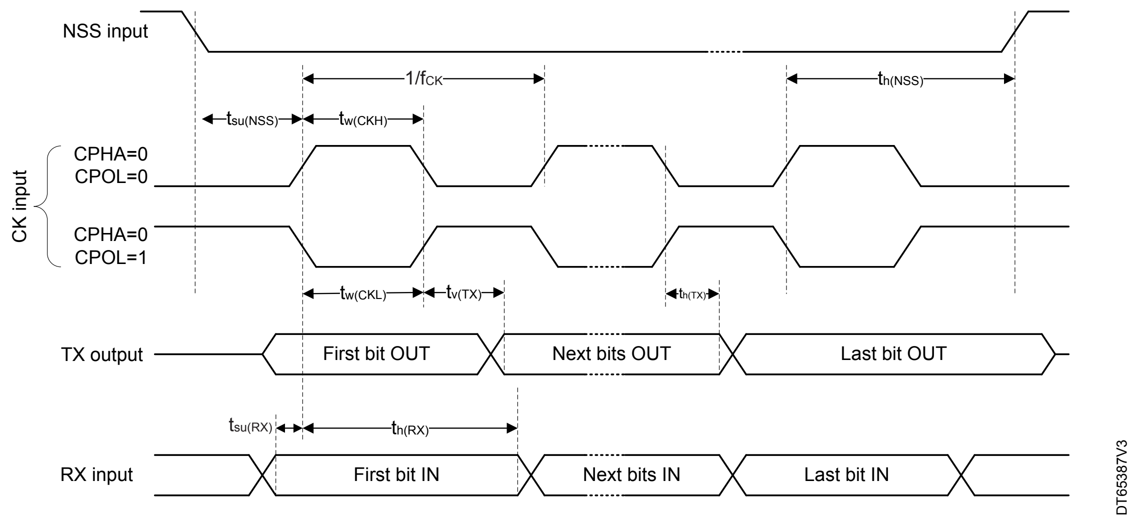


Figure 28. USART timing diagram in SPI slave mode



6.3.27 SPI characteristics

Unless otherwise specified, the parameters given in Table 83 for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 83. SPI characteristics

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode receiver/full duplex 1.71 < V_{DD} < 3.6 V Voltage Range 1	-	-	27	MHz
		Master mode transmitter 1.71 < V_{DD} < 3.6 V Voltage Range 1			27	
		Slave mode receiver 1.71 < V_{DD} < 3.6 V Voltage Range 1			27	
		Slave mode transmitter/full duplex 2.7 < V_{DD} < 3.6 V Voltage Range 1			27(1)	
		Slave mode transmitter/full duplex 1.71 < V_{DD} < 3.6 V Voltage Range 1			21.5(1)	
		Voltage Range 2			9.5	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	4	-	-	T_{PCLK}
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	2	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{SCK2} - 1.5(2)	T_{SCK2}(2)	T_{SCK2} + 1.5(2)	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	ns
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2.5	-	-	ns
$t_{h(SI)}$		Slave mode	2.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	12.5	20	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	6	7.5	18	ns
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 < V_{DD} < 3.6 V Voltage Range 1	-	15	18	ns
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 1	-	15	23	
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 2	-	22	30	
$t_{v(MO)}$		Master mode	-	3	5.5	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	ns
$t_{h(MO)}$		Master mode	1	-	-	

1. *Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.*
2. *$T_{SCK2} = T_{PCLK} \times prescaler / 2$*

Figure 29. SPI timing diagram - slave mode and CPHA = 0

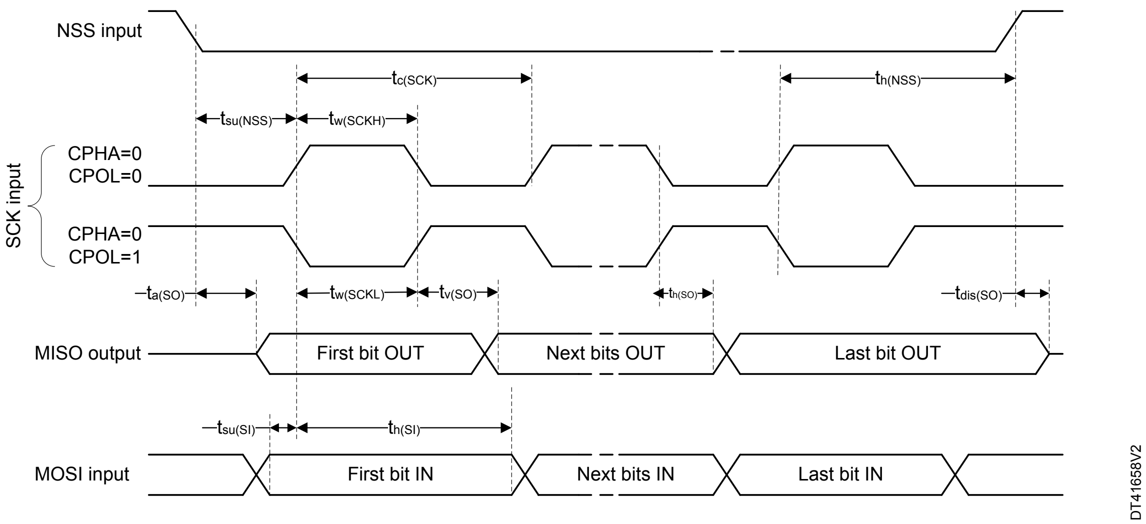
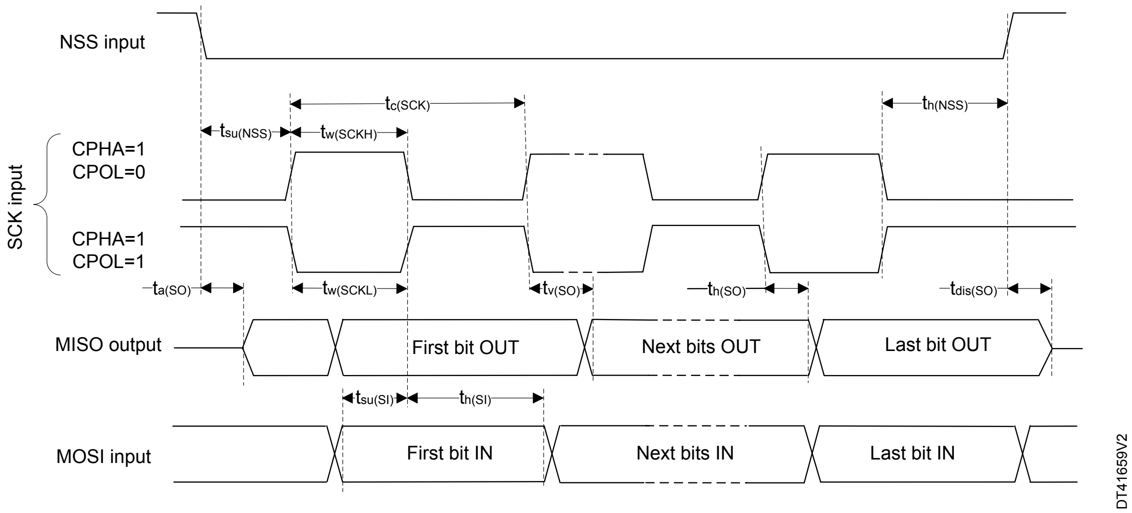
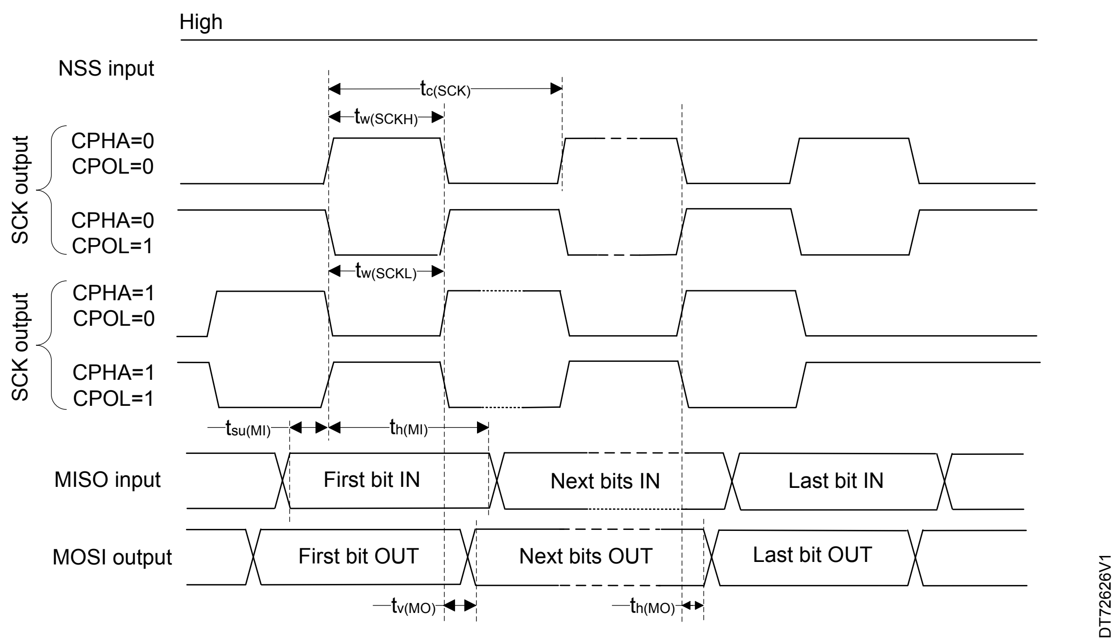


Figure 30. SPI timing diagram - slave mode and CPHA = 1



1. *Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.*

Figure 31. SPI timing diagram - master mode



1. *Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.*

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

The WLCSP27 package information is under definition.

7.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

7.2 TSSOP20 package information (YA)

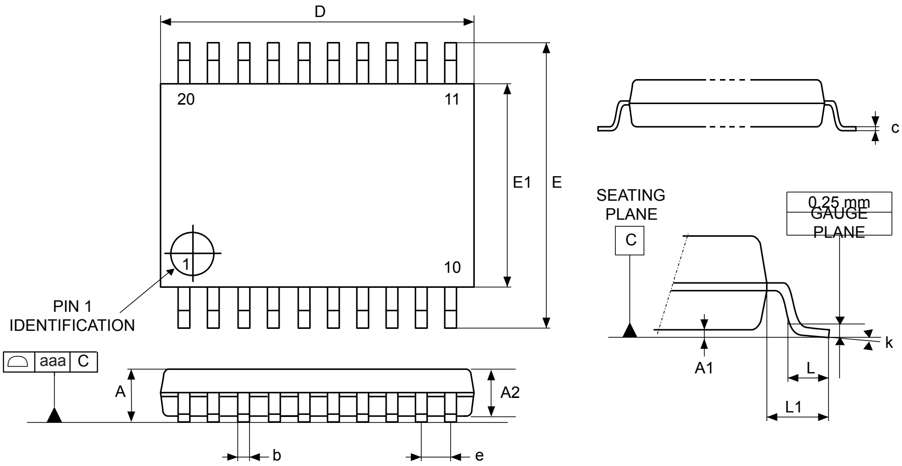


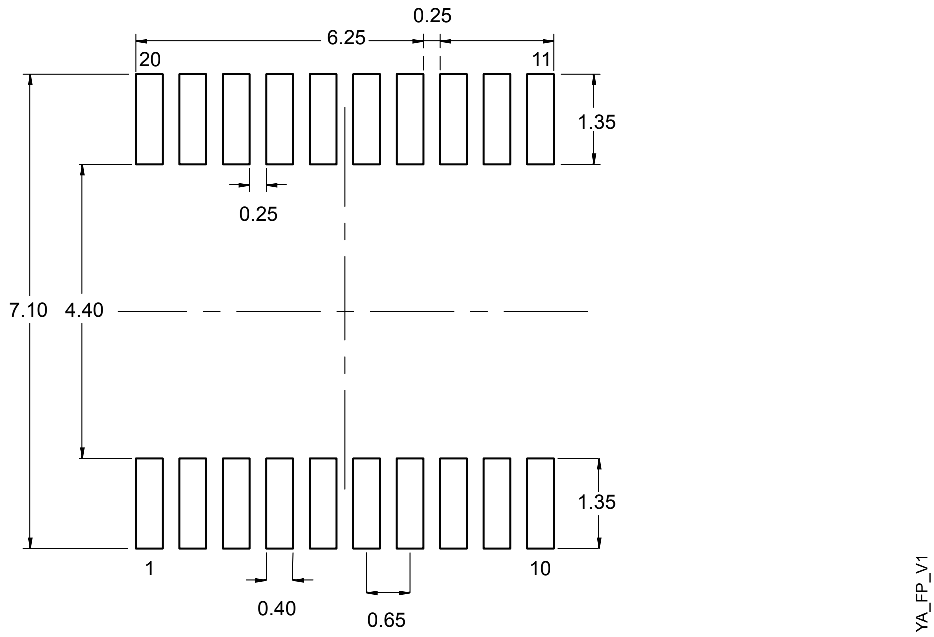
Figure 32. TSSOP20 - Outline

Table 84. TSSOP20 - Mechanical data

Symbol	Millimeters			Inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.2	-	-	0.0472
A1	0.05	-	0.15	0.002	-	0.0059
A2	0.8	1	1.05	0.0315	0.0394	0.0413
b	0.19	-	0.3	0.0075	-	0.0118
c	0.09	-	0.2	0.0035	-	0.0079
D	6.4	6.5	6.6	0.252	0.2559	0.2598
E	6.2	6.4	6.6	0.2441	0.252	0.2598
E1	4.3	4.4	4.5	0.1693	0.1732	0.1772
e	-	0.65	-	-	0.0256	-
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1	-	1	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.1	-	-	0.0039

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

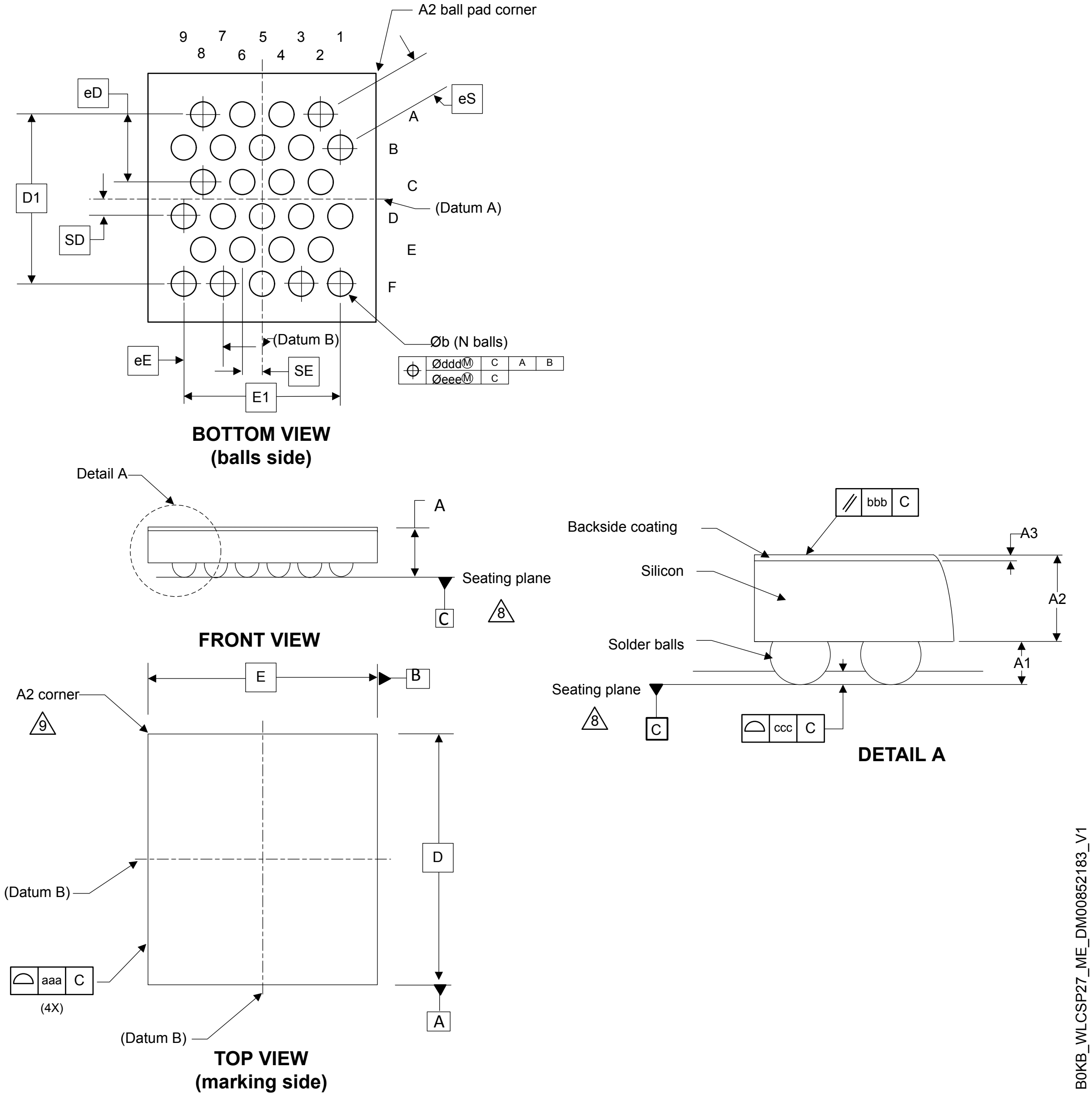
Figure 33. TSSOP20 - Footprint example



7.3 WLCSP27 package information (B0KB)

This WLCSP is a 27-ball, 2.55 x 2.34 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 34. WLCSP27 - Outline



1. *Drawing is not to scale*

Table 85. WLCSP27 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.58	-	-	0.0228
A1[3]	-	0.17	-	-	0.0067	-
A2	-	0.38	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b[4]	0.23	0.25	0.28	0.0091	0.0098	0.0110
D[5]	2.55 BSC			0.1004 BSC		
D1[5]	1.732 BSC			0.0682 BSC		
E[5]	2.340 BSC			0.0921 BSC		
E1[5]	1.600 BSC			0.0630 BSC		
eD[5][6]	0.693 BSC			0.0273 BSC		
eE[5][6]	0.400 BSC			0.0157 BSC		
N[7]	27					
SD[5][8]	0.173 BSC			0.0068 BSC		
SE[5][8]	0.200 BSC			0.0079		
aaa[9]	0.030			0.0012		
bbb[9]	0.060			0.0024		
ccc[9]	0.030			0.0012		
ddd[9]	0.015			0.0006		
eee[9]	0.050			0.0020		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height A is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to Datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances, refer to form and position table. On the drawing, these dimensions are framed. For the tolerances, refer to form and position values.*
6. *e represents the solder balls grid pitch(es).*
7. *N represents the total number of balls.*
8. *Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.*
9. *Tolerance of form and position drawing*

Figure 35. **WLCSP27 - Footprint example**

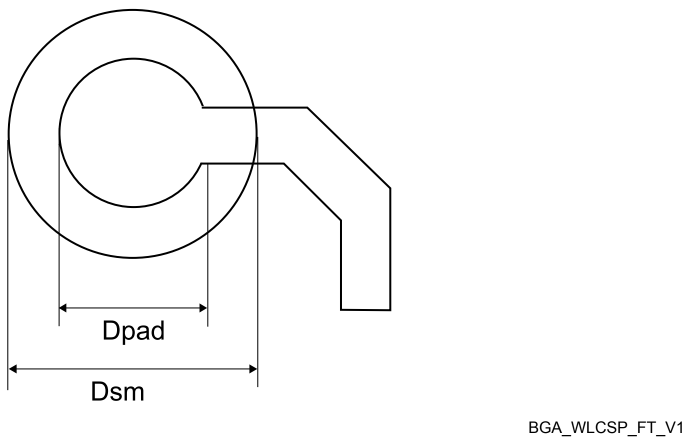


Table 86. **WLCSP27 - Example of PCB design rules**

Dimension	Values
Pitch	0.400 mm
Dpad	0.250 mm
Dsm	0.325 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.325 mm
Stencil thickness	0.100 mm

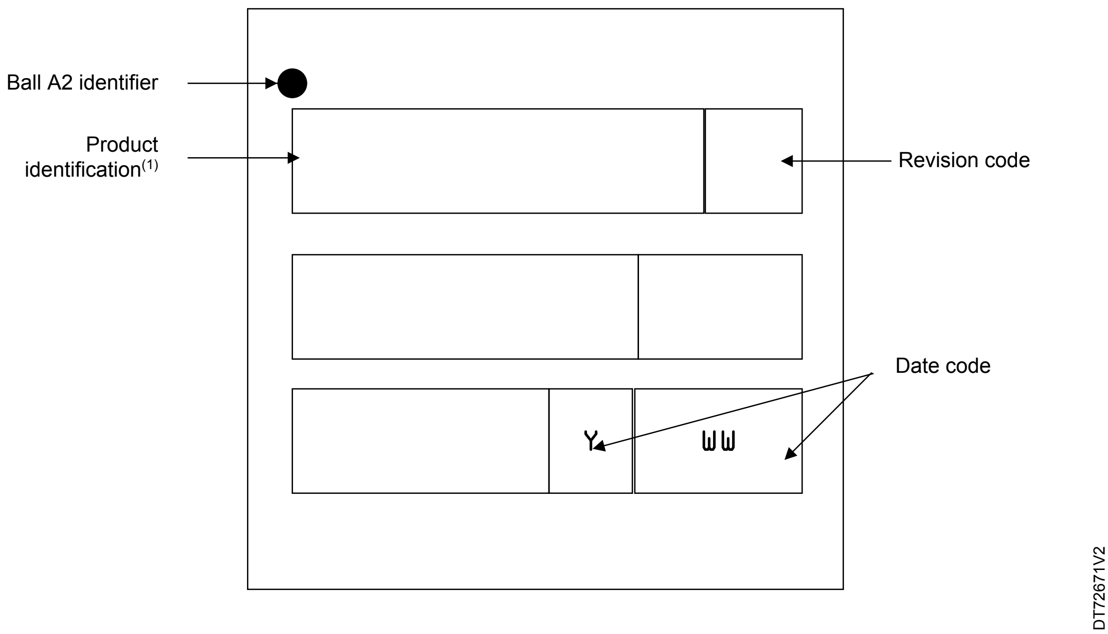
7.3.1 Device marking for WLCSP27

The following figure gives an example of topside marking versus ball A2 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 36. **WLCSP27 marking example**

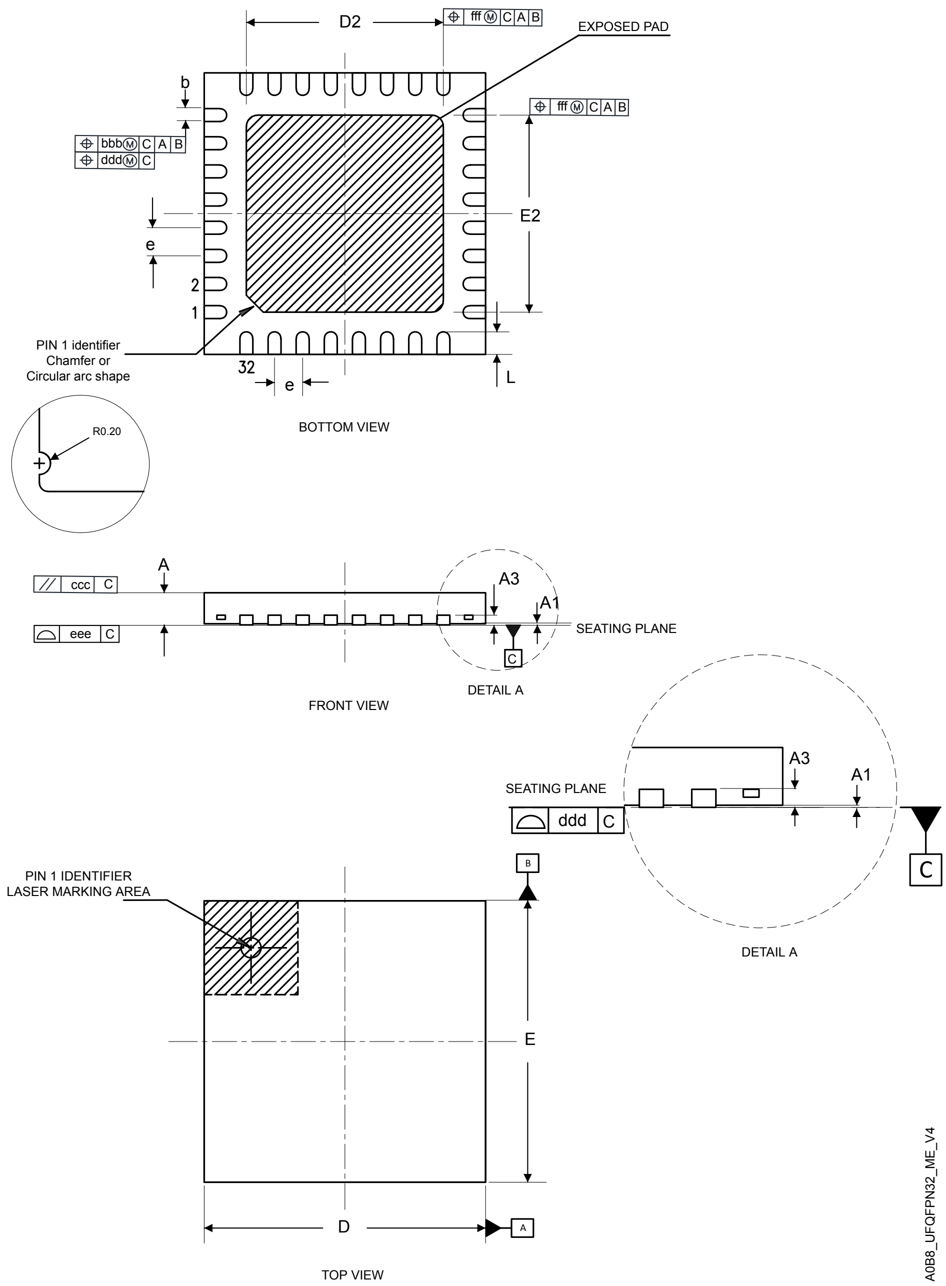


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 UFQFPN32 package information (A0B8)

This UFQFPN is a 32 pins, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package.

Figure 37. UFQFPN32 - Outline



1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.*

Table 87. UFQFPN32 - Mechanical data

Symbol	millimeters(1)			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A(3)(4)	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1(5)	0.00	-	0.05	0.000	-	0.0020
A3(6)	-	0.15	-	-	0.0060	-
b(7)	0.18	0.25	0.30	0.0071	0.010	0.0118
D(8)(9)	5.00 BSC			0.1969 BSC		
D2	3.50	3.60	3.70	0.139	0.143	0.147
E(8)(9)	5.00 BSC			0.1969 BSC		
E2	3.50	3.60	3.70	0.139	0.143	0.147
e(9)	-	0.50	-	-	0.02	-
N(10)	32					
K	0.15	-	-	0.006	-	-
L	0.30	-	0.50	0.0119	-	0.0199
R	0.09	-	-	0.004	-	-

1. *All dimensions are in millimetres. Dimensioning and tolerancing schemes are conform to ASME Y14.5M-2018 except European .*
2. *Values in inches are converted from mm and rounded to 4 decimal digits.*
3. *UFQFPN stands for Ultra thin Fine pitch Quad Flat Package No lead: A ≤ 0.60mm / Fine pitch e ≤ 1.00mm.*
4. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
5. *A1 is the vertical distance from the bottom surface of the plastic body to the nearest metallized package feature.*
6. *A3 is the distance from the seating plane to the upper surface of the terminals.*
7. *Dimension b applies to metallized terminal. If the terminal has the optional radius on the other end of the terminal, the dimension b must not be measured in that radius area.*
8. *Dimensions D and E do not include mold protrusion, not to exceed 0,15mm.*
9. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to Table 88*
10. *N represents the total number of terminals.*

Table 88. Tolerance of form and position

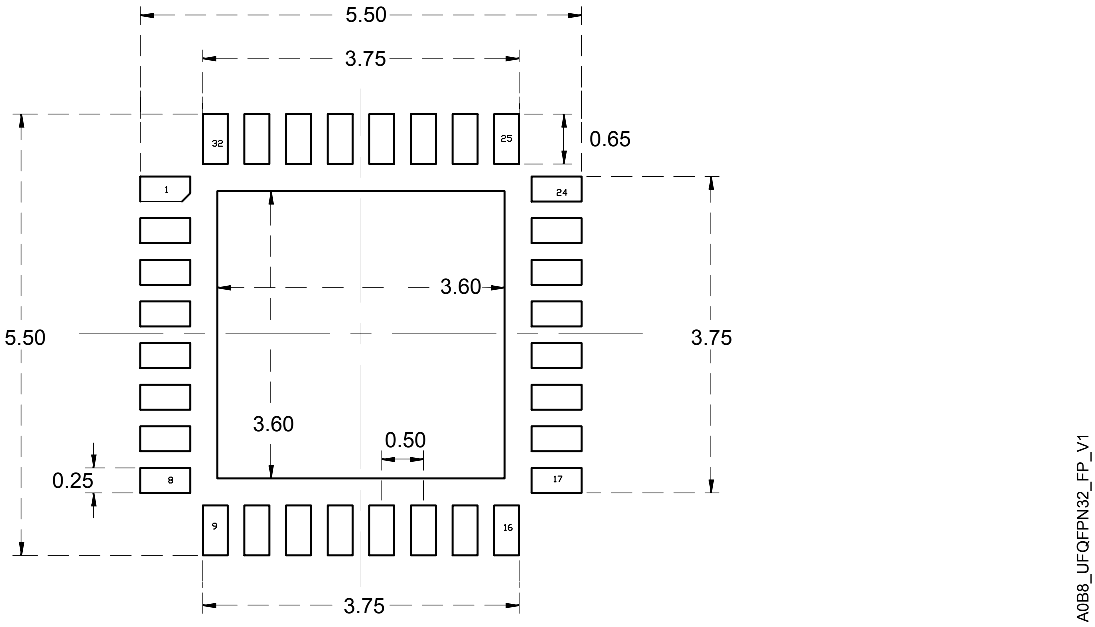
Symbol(1)	Tolerance of form and position(2) In millimeters	Tolerance of form and position(3) In inches
aaa	0.15	0.006
bbb	0.10	0.004
ccc	0.10	0.004
ddd	0.05	0.002
eee	0.10	0.004
fff	0.10	0.004

1. *For the tolerance of form and position definitions see Table 89.*
2. *All dimensions are in millimetres. Dimensioning and tolerancing schemes are conform to ASME Y14.5M-2018 except European .*
3. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Table 89. **Tolerance of form and position symbol definition**

Symbol	Definition
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centres of the profile zones are defined by the basic dimensions D and E.
bbb	The tolerance that controls the position of the terminals with respect to Datums A and B. The centre of the tolerance zone for each terminal is defined by basic dimension e as related to datums A and B.
ccc	The tolerance located parallel to the seating plane in which the top surface of the package must be located.
ddd	The tolerance that controls the position of the terminals to each other. The centres of the profile zones are defined by basic dimension e.
eee	The unilateral tolerance located above the seating plane wherein the bottom surface of all terminals must be located = coplanarity
fff	The tolerance that controls the position of the exposed metal heat feature. The centre of the tolerance zone is the data defined by the centrelines of the package body

Figure 38. **UFQFPN32 - Footprint example**



1. *Dimensions are expressed in millimeters.*

7.5 LQFP48 package information (5B)

This LQFP is a 48-pins, 7 x 7 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

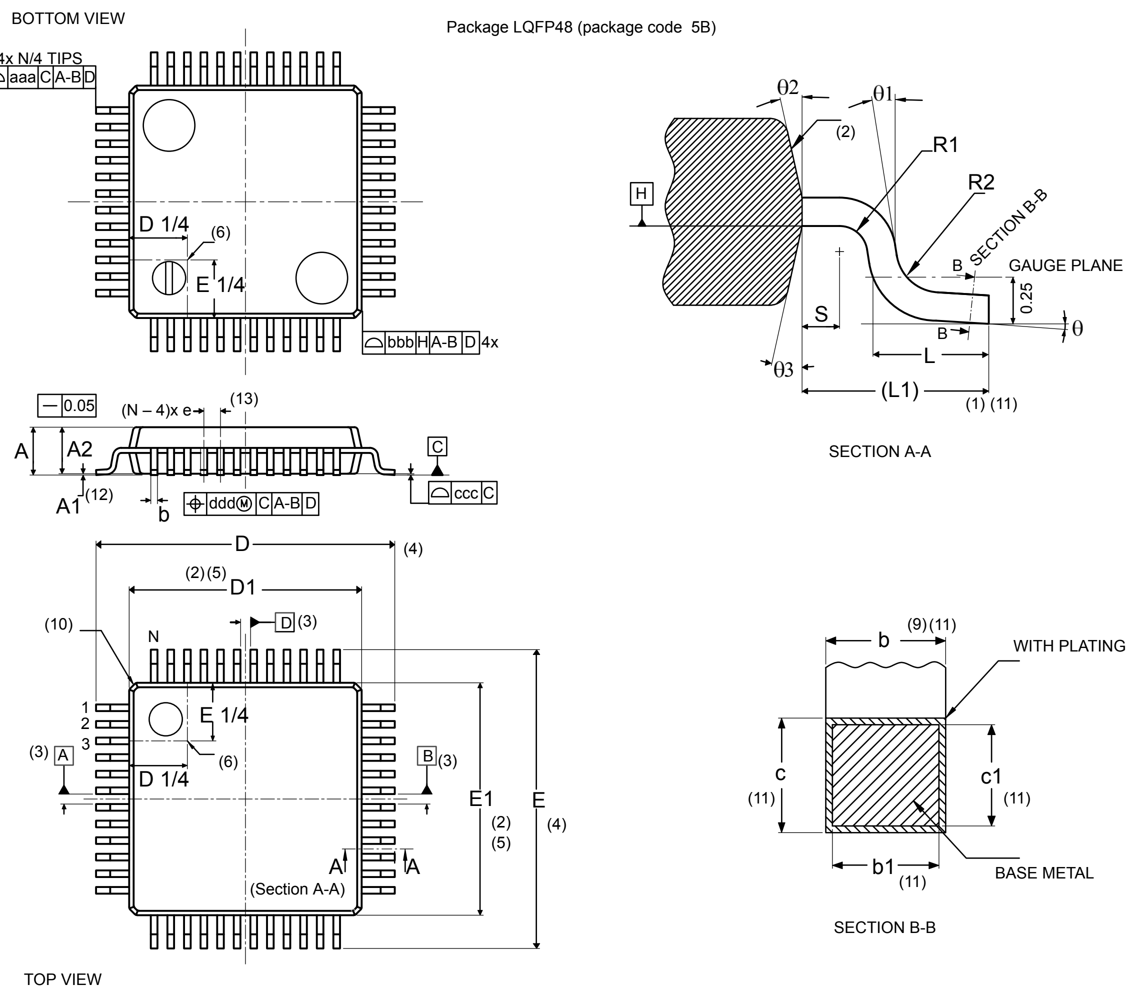


Figure 39. LQFP48- Outline[15.]

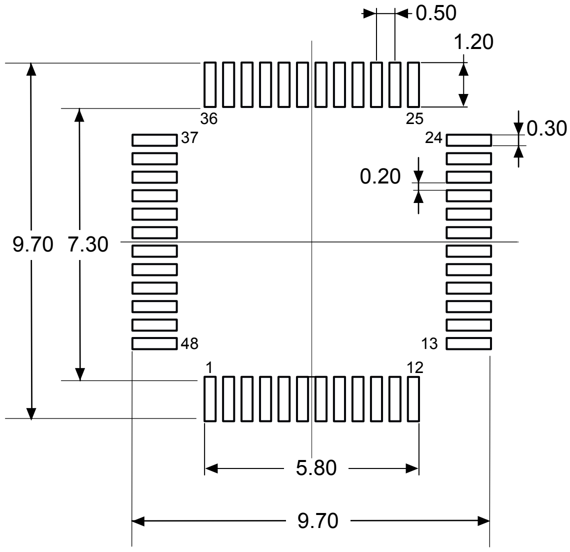
Table 90. LQFP48 - Mechanical data

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
D[4.]	9.00 BSC			0.3543 BSC		
D1[4.][5.]	7.00 BSC			0.2756 BSC		
E[4.]	9.00 BSC			0.3543 BSC		
E1[4.][5.]	7.00 BSC			0.2756 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13.]	48					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.][7.]	0.20			0.0079		
bbb[1.][7.]	0.20			0.0079		
ccc[1.][7.]	0.08			0.0031		
ddd[1.][7.]	0.08			0.0031		

Notes:
1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits
15. Drawing is not to scale.

Figure 40. LQFP48 - Footprint example

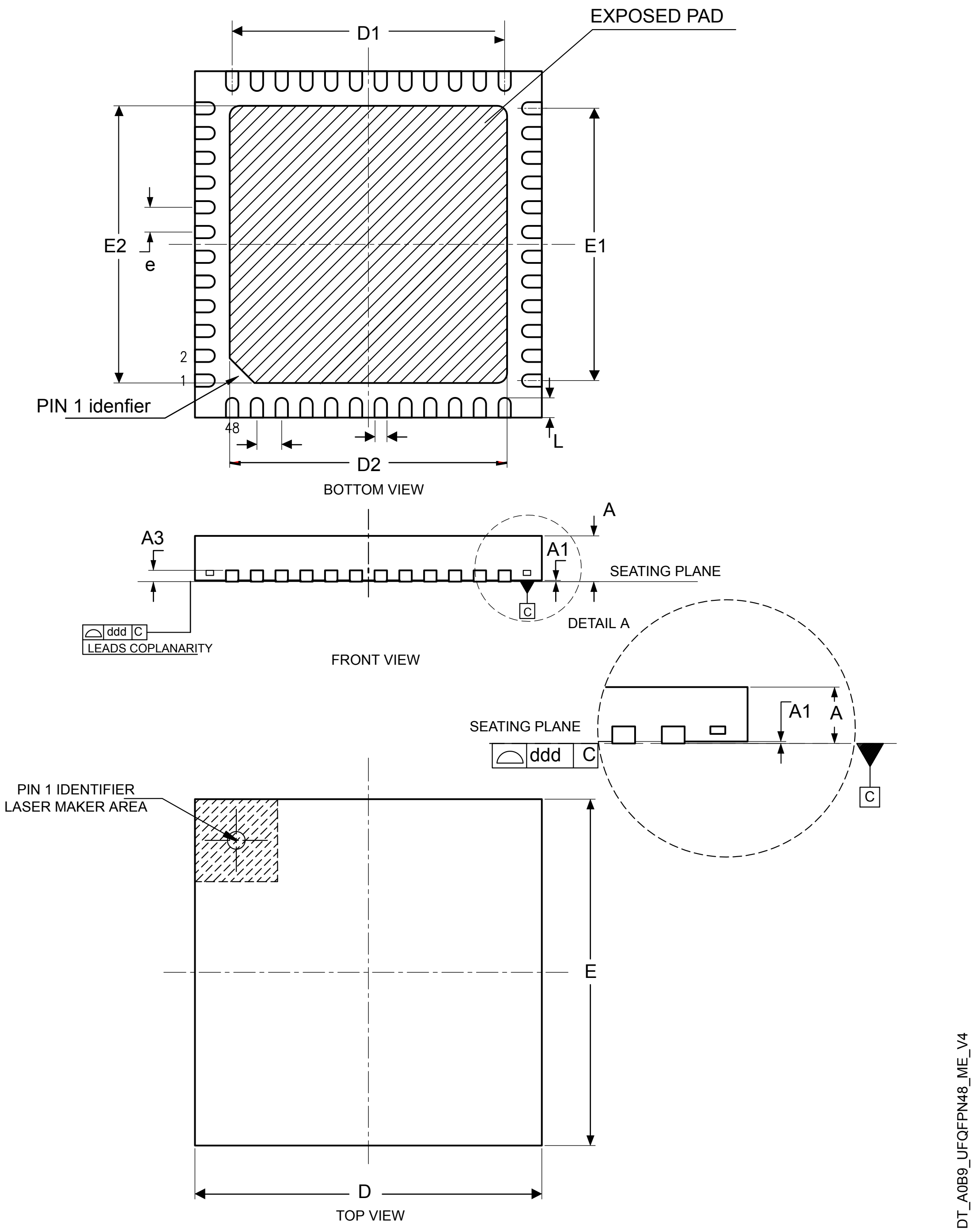


1. *Dimensions are expressed in millimeters.*

7.6 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 41. UFQFPN48 - Outline



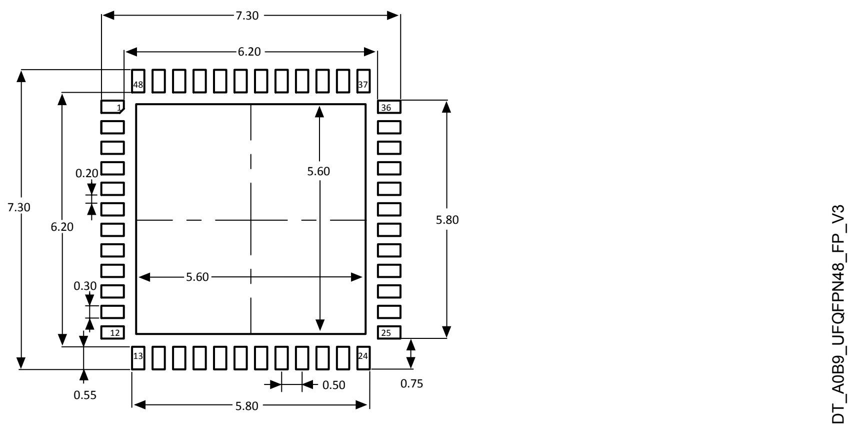
1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the under side of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.*

Table 91. **UFQFPN48 - Mechanical data**

Symbol	Millimeters			Inches (1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D(2)	6.900	7.000	7.100	0.2717	0.2756	0.2795
D1	5.400	5.500	5.600	0.2126	0.2165	0.2205
D2(3)	5.500	5.600	5.700	0.2165	0.2205	0.2244
E(2)	6.900	7.000	7.100	0.2717	0.2756	0.2795
E1	5.400	5.500	5.600	0.2126	0.2165	0.2205
E2(3)	5.500	5.600	5.700	0.2165	0.2205	0.2244
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.*
3. *Dimensions D2 and E2 are not in accordance with JEDEC.*

Figure 42. **UFQFPN48 - Footprint example**



1. *Dimensions are expressed in millimeters.*

7.7 LQFP64 package information (5W)

This is a 64-pins, 10 x 10 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 43. **LQFP64 - Outline**(15.)

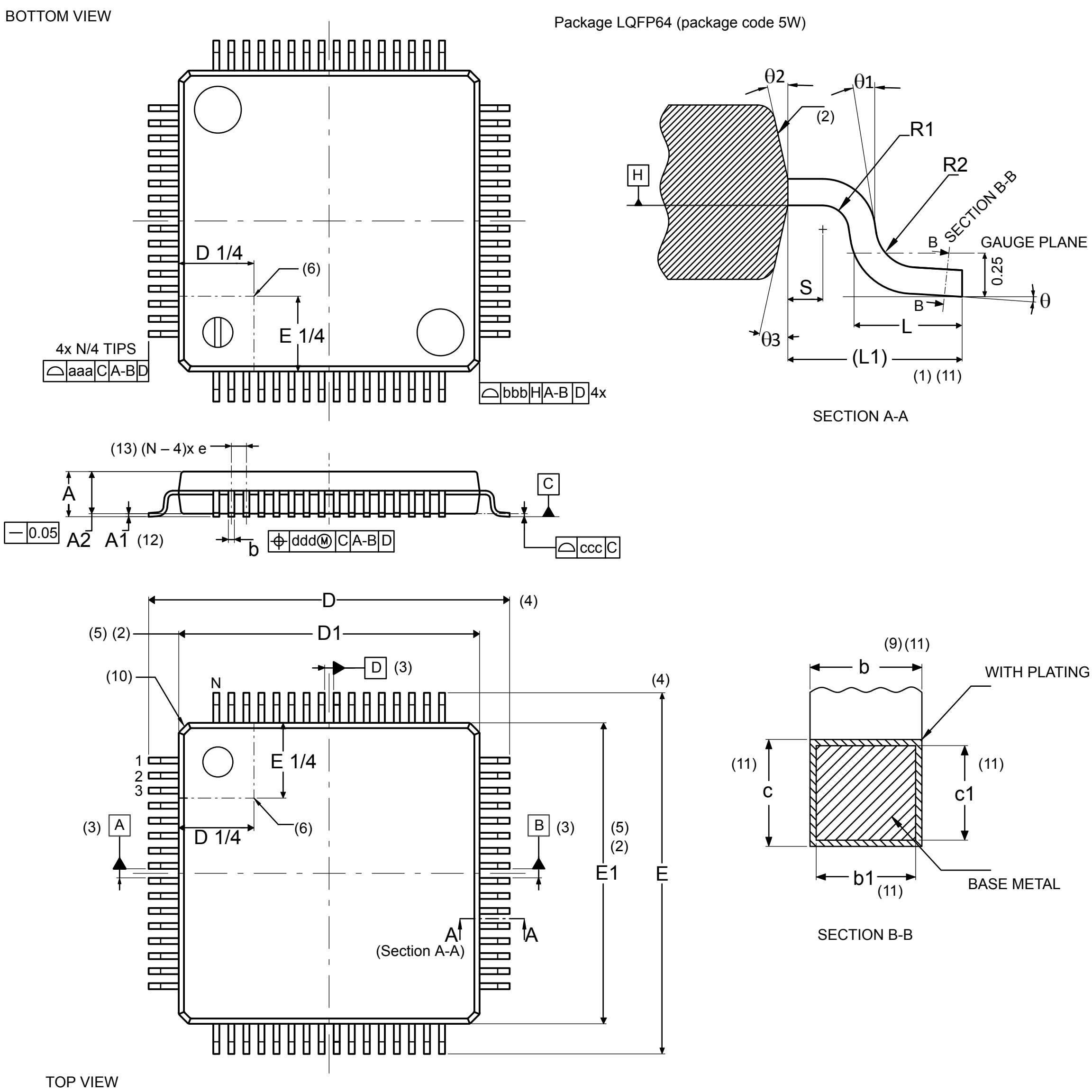


Table 92. **LQFP64 - Mechanical data**

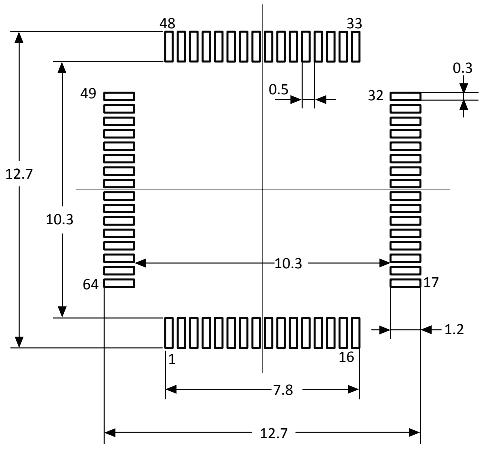
Symbol	millimeters			inches(14.)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1(12.)	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b(9.)(11.)	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1(11.)	0.17	0.20	0.23	00067	0.0079	0.0091

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	12.00 BSC			0.4724 BSC		
D1[2.][5.]	10.00 BSC			0.3937 BSC		
E[4.]	12.00 BSC			0.4724 BSC		
E1[2.][5.]	10.00 BSC			0.3937 BSC		
e	0.500 BSC			0.0197 BSC		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
N[13.]	64					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]	0.20			0.0079		
bbb[1.]	0.20			0.0079		
ccc[1.]	0.08			0.0031		
ddd[1.]	0.08			0.0031		

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 44. LQFP64 - Footprint example



1. *Dimensions are expressed in millimeters.*

7.8 UFBGA64 package information (A019)

This UFBGA is a 64-ball, 5 x 5 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 45. UFBGA64 - Outline[13.]

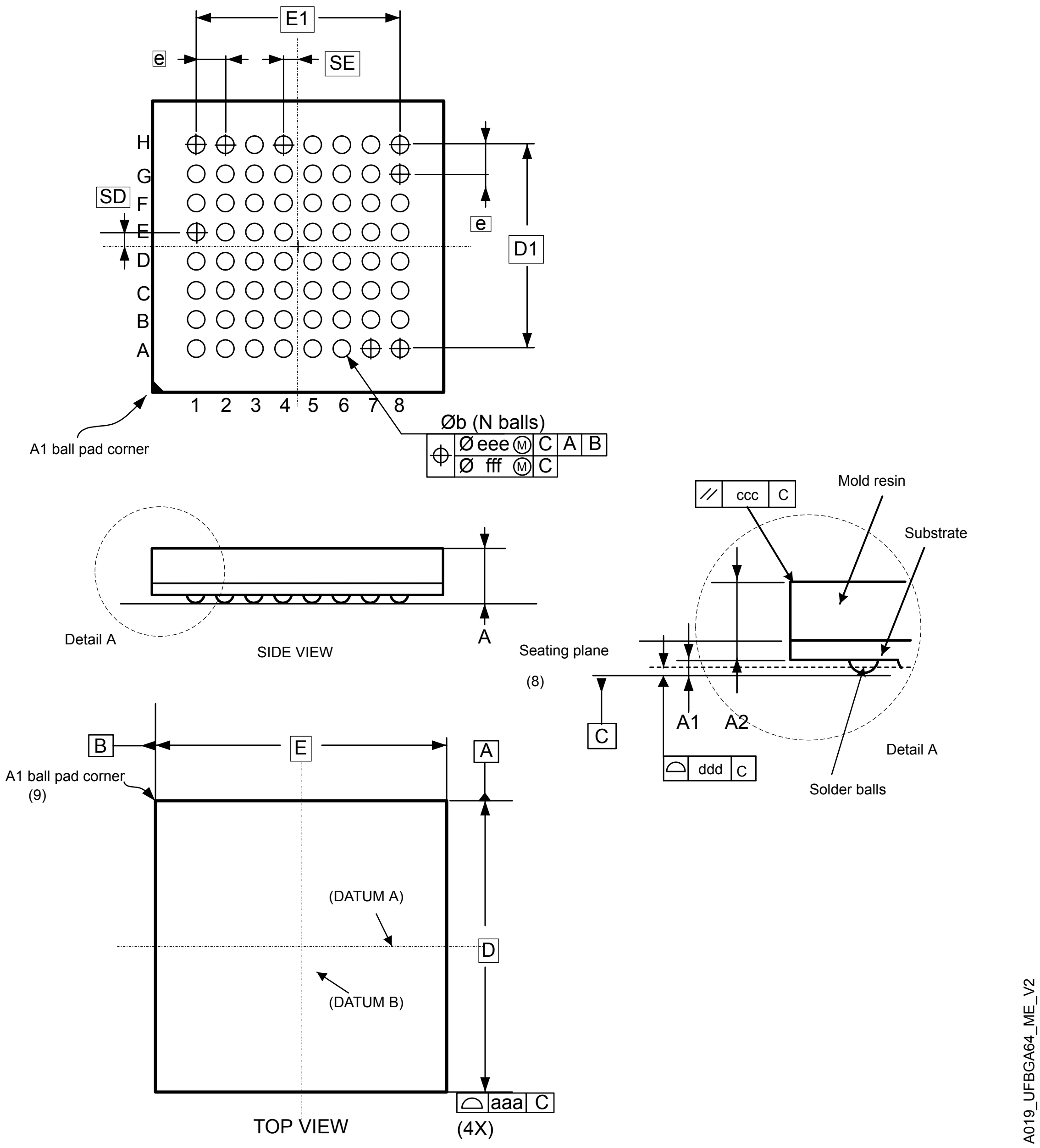


Table 93. UFBGA64 - Mechanical data

Symbol	millimeters[1.]			inches [12.]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2.][3.]	-	-	0.60	-	-	0.0236
A1[4.]	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-

Symbol	millimeters[1.]			inches [12.]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b[5.]	0.23	0.28	0.33	0.0090	0.0110	0.0130
D[6.]	5.00 BSC			0.1969 BSC		
D1	3.50 BSC			0.1378 BSC		
E	5.00 BSC			0.1969 BSC		
E1	3.50 BSC			0.1378 BSC		
e[9.]	0.50 BSC			0.0197 BSC		
N[10.]	64					
SD[11.]	0.25 BSC			0.0098 BSC		
SE[11.]	0.25 BSC			0.0098 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.05			0.0020		

Notes:
1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ultra profile fine pitch ball grid array: 0.50 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale

Figure 46. UFBGA64 - Footprint example

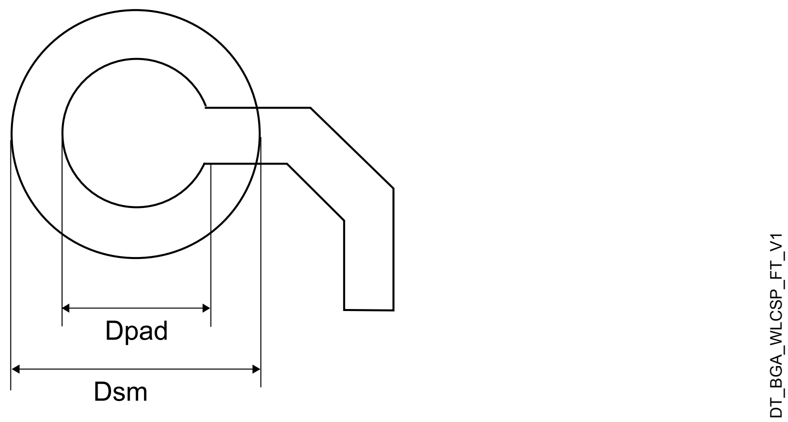


Table 94. UFBGA64 - Recommended PCB design rules (0.50 mm pitch BGA)

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm aperture diameter
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

7.9 Package thermal characteristics

The operating junction temperature, T_J, must never exceed the maximum given in Section 6.3.1: General operating conditions.

The maximum junction temperature in °C that the device can reach if respecting the operating conditions, is: operating conditions, is:

$$T_J \max = T_A \max + \left(P_D \max \times \Theta_{JA}\right)$$

where:

- T_{Amax} is the maximum ambient temperature, in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.
- $P_D = P_{INT} + P_{I/O}$
  - P_{INT} is the power dissipation contribution from product to I_{DD} and V_{DD}, expressed in Watts.
  - $P_{I/O}$ is the power dissipation contribution from output ports where: $P_{I/O} = \sum\left(V_{OL} \times I_{OL}\right) + \sum\left(\left(V_{DDIOx} - V_{OH}\right)\right) \times I_{OH}$ taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 95. Package thermal characteristics

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	TSSOP20	78.5	°C/W
		WLCSP27	78.0	
		UFQFPN32	41.2	
		LQFP48	53.2	

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	UFQFPN48	30.7	°C/W
		LQFP64	46.2	
		UFBGA64	60.4	
Θ_{JB}	Thermal resistance junction-board	TSSOP20	49.4	
		WLCSP27	50.8	
		UFQFPN32	23.1	
		LQFP48	30.5	
		UFQFPN48	15.0	
		LQFP64	28.6	
		UFBGA64	43.6	
Θ_{JC}	Thermal resistance junction-top case	TSSOP20	24.8	
		WLCSP27	5.3	
		UFQFPN32	19.0	
		LQFP48	18.6	
		UFQFPN48	11.6	
		LQFP64	15.9	
		UFBGA64	19.2	

7.9.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air) available on www.jedec.org.
- For information on thermal management, refer to application note *"Guidelines for thermal management on STM32 applications" (AN5036)* available on www.st.com.

8 Ordering information

Example:	STM32	U	031	K	C	T	6	TR

Device family

STM32 = Arm®-based 32-bit microcontroller

Product type

U = Ultra-low-power

Device subfamily

031 = STM32U031xx

Pin count

F = 20 pins

G = 27 balls

K = 32 pins

C = 48 pins

R = 64 pins/balls

Flash memory size

4 = 16 Kbytes of flash memory

6 = 32 Kbytes of flash memory

8 = 64 Kbytes of flash memory

Package

P = TSSOP ECOPACK2

T = LQFP ECOPACK2

U = UFQFPN ECOPACK2

I = UFBGA ECOPACK2

Y = WLCSP ECOPACK2

Temperature range

3 = Industrial temperature range, –40 to 125 °C (130 °C junction)

6 = Industrial temperature range, –40 to 85°C (105 °C junction)

Packing

TR = Tape and reel

xxx = Programmed parts

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on www.st.com for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
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Revision history

Table 96. Document revision history

Date	Revision	Changes
01-Mar-2024	1	Initial release.
18-Mar-2024	2	Cover page: • Updated ULPMark™-CP and ULPMark™-PP values on cover page. • Changed number of touch sensing channel to 18. Added Section 3.19: Touch sensing controller (TSC). Updated $I_{DD\ (Stop\ 1)}$ maximum values in Table 38. Current consumption in Stop 1 mode. Added $I_{DD\ (Stop\ 2)}$ maximum values in Table 39. Current consumption in Stop 2 mode. Added $I_{DD\ (SRAM2)}$ maximum values in Table 40. Current consumption in Standby mode.

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