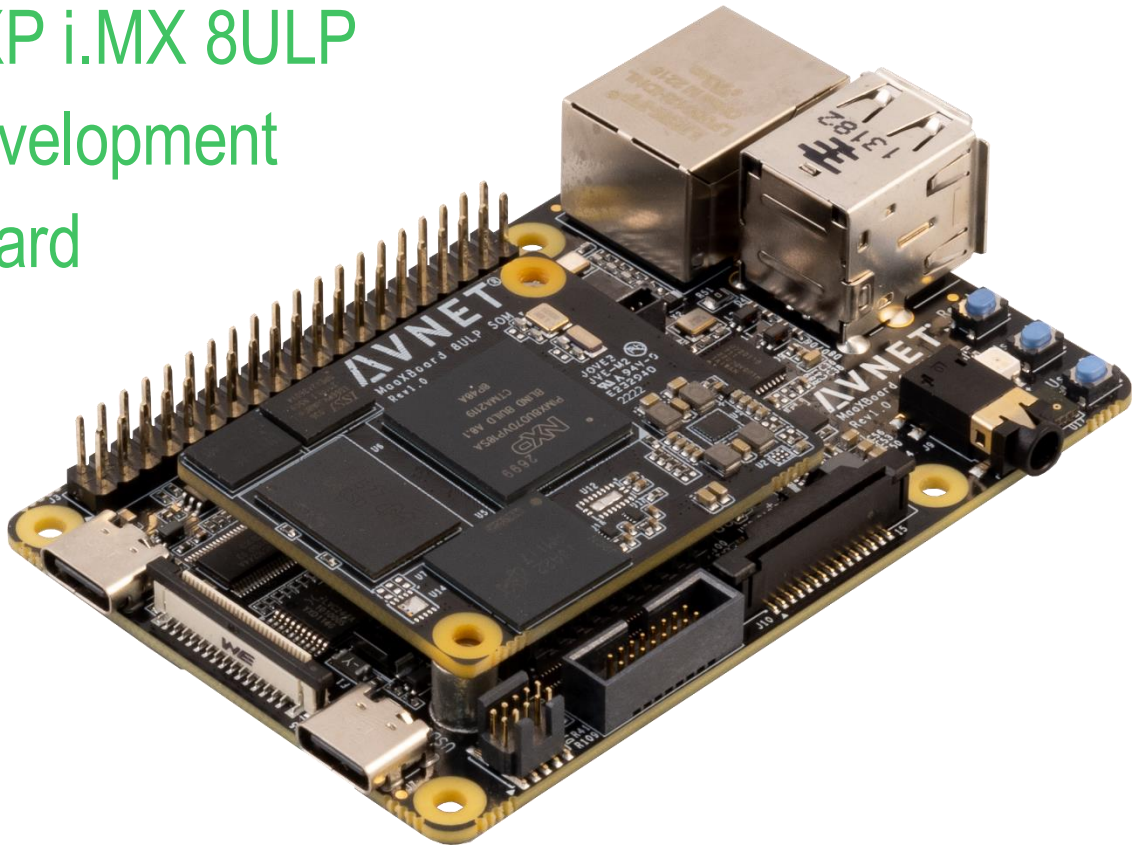
Ultra-Low Power
NXP i.MX 8ULP
Development
Board



MaaXBoard 8ULP
Hardware User Guide

v1.0 October 03, 2023

1 Document Control

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2 Version History

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1.0	10/03/2023	Initial release

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3 Hardware Checklist

Hardware items recommended for application development are the following

#	Item Description
1	Computer (Windows / Linux / Mac) with installed development tools (see below)
2	Avnet MaaXBoard 8ULP board http://avnet.me/MaaXBoard-8ULP
3	NXP MCU-LINK Debugger/Programmer Probe (plus USB type-A to MicroUSB cable)
4	5V 2A power adapter (plus USB type-A to USB type-C cable)
5	USB current monitor dongle *(optional)*
6	MaaXBoard MIPI-DSI 7" Capacitive Touch 720 x 1280 Display *(optional)* p/n: AES-ACC-MAAX-DISP2
7	MIPI-CSI Camera, 5 MP, OV5640 image sensor *(optional)* p/n: Arducam B0470 camera

Table 1 – Hardware Checklist

4 Software Checklist

Listed below are the software items mentioned in this document

#	Item Description
1	**Visual Studio Code IDE** https://code.visualstudio.com/download
2	**NXP MCUXpresso SDK** (SDK_2.14.1_EVK-MIMX8ULP or later) Search by name: "**8ULP-EVK**" on NXP SDK builder site at: https://mcuxpresso.nxp.com/en/select Select **MIMX8ULP-EVK** then click **Build MCUXpresso SDK_2.14.1_EVK-MIMX8ULP** to download
3	Avnet MaaXBoard 8ULP pre-built Boot image and MaaXBoard 8ULP pre-built Linux BSP image

Table 2 – Software Checklist

5 Introduction

MaaXBoard 8ULP has been engineered as two PCBs:

- a small SOM (43mm x 36mm) fitted via 2x100-pin connectors onto
- a compact Raspberry Pi form-factor baseboard (85mm x 56mm)

The baseboard supports multiple communication-, UI and vison interfaces, including:

- 2x USB 2.0 Host and 1x USB 2.0 device interfaces
- 1x 100M Ethernet
- Wi-Fi 5 / BT5.1 wireless M.2 module + U.FL external antenna (optional)
- MIPI DSI touchscreen display interface (4 lane)
- MIPI CSI camera interface (2 lane)

Audio and voice UI applications are supported via onboard:

- Stereo audio codec
- Stereo headphone jack and single digital microphone

Three sets of expansion headers further extend the board's capabilities:

- a Pi-HAT compatible 40-pin header,
- a MikroE Click 16-pin header
- an ADC/DAC 6-pin header.

The board's unique debug subsystem supports remote USB access to:

- Three UARTs (for A35 #0, A35 #1 and M33 debug interfaces)
- I/O expander-based remote control & monitoring (16 signals)
- integrated SWD/JTAG debugger interface (or external 10pin header)

On rear of the board an M.2 connector facilitates addition of a Wi-Fi 5 + Bluetooth 5.1 wireless module.

The i.MX 8ULP device on this board is architected with 3 separated processor power domains:

- Application domain includes two Arm® Cortex®-A35 (800 MHz) cores plus 3D/2D GPUs
- Real Time domain includes an Arm Cortex-M33 (216 MHz) core, plus Fusion DSP (200 MHz) core
- LPAV domain (Low Power Audio Video) has a HiFi 4 DSP (475 MHz)

The i.MX8ULP is also differentiated from other processor solutions by it's:

- Large amount of OCRAM (896 KB)
- Advanced EdgeLock® security enclave .

Input power (+5V) is sourced via the USB-C Device connector (or the R-Pi header pins) and is managed via NXP's PCA9460B PMIC on the SOM plus three additional voltage regulators.

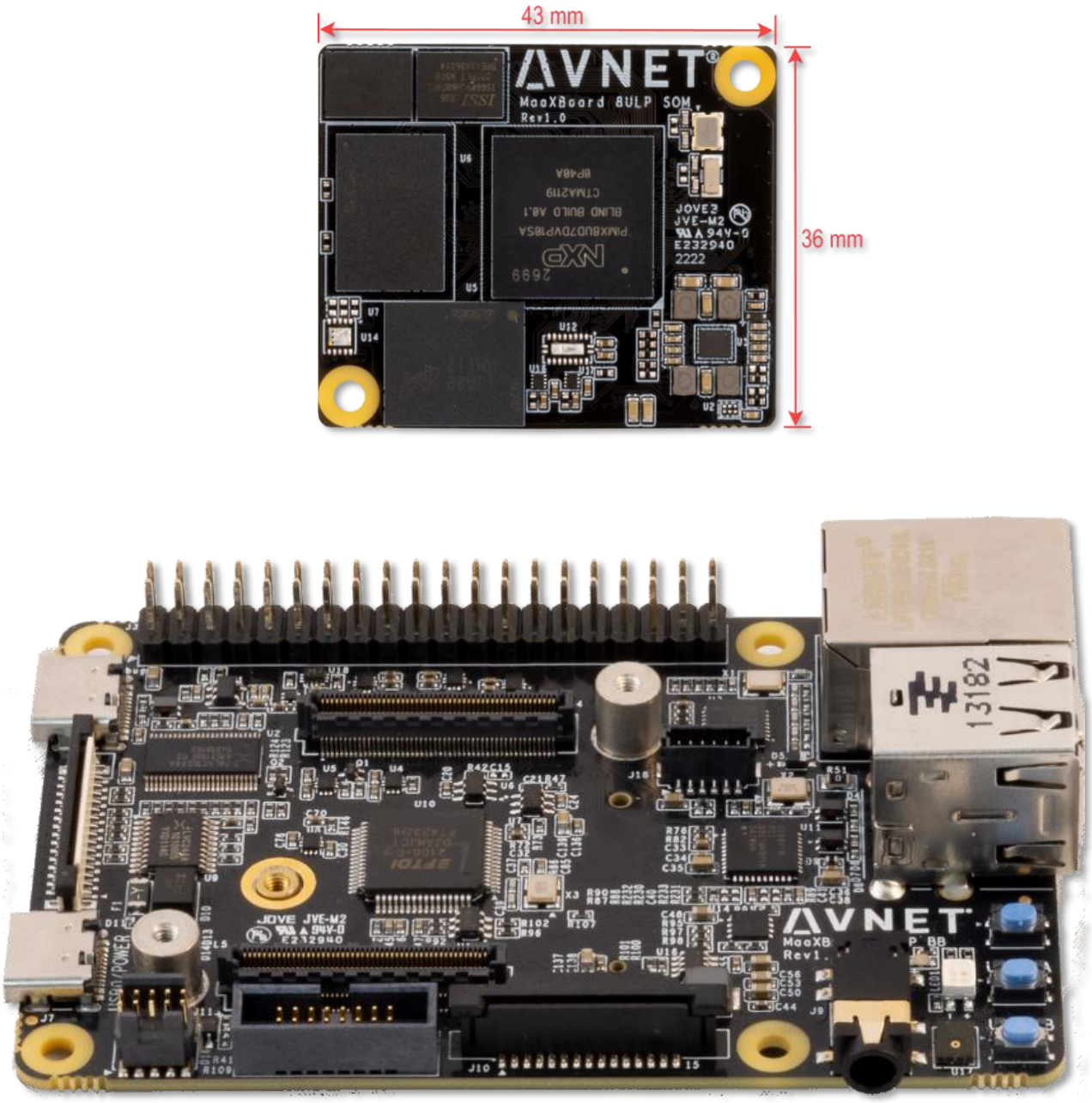


Figure 1 – MaaXBoard 8ULP Baseboard (BB) and Compute Module (SOM

5.1 MaaXBoard 8ULP Info

- Part# to order: AES-MAAXB-8ULP-SK-G
- Product Page: http://avnet.me/MaaXBoard-8ULP

5.2 Items Included with MaaXBoard 8ULP

- MaaXBoard 8ULP board
- QuickStart Card
- Downloadable examples, reference designs and documentation

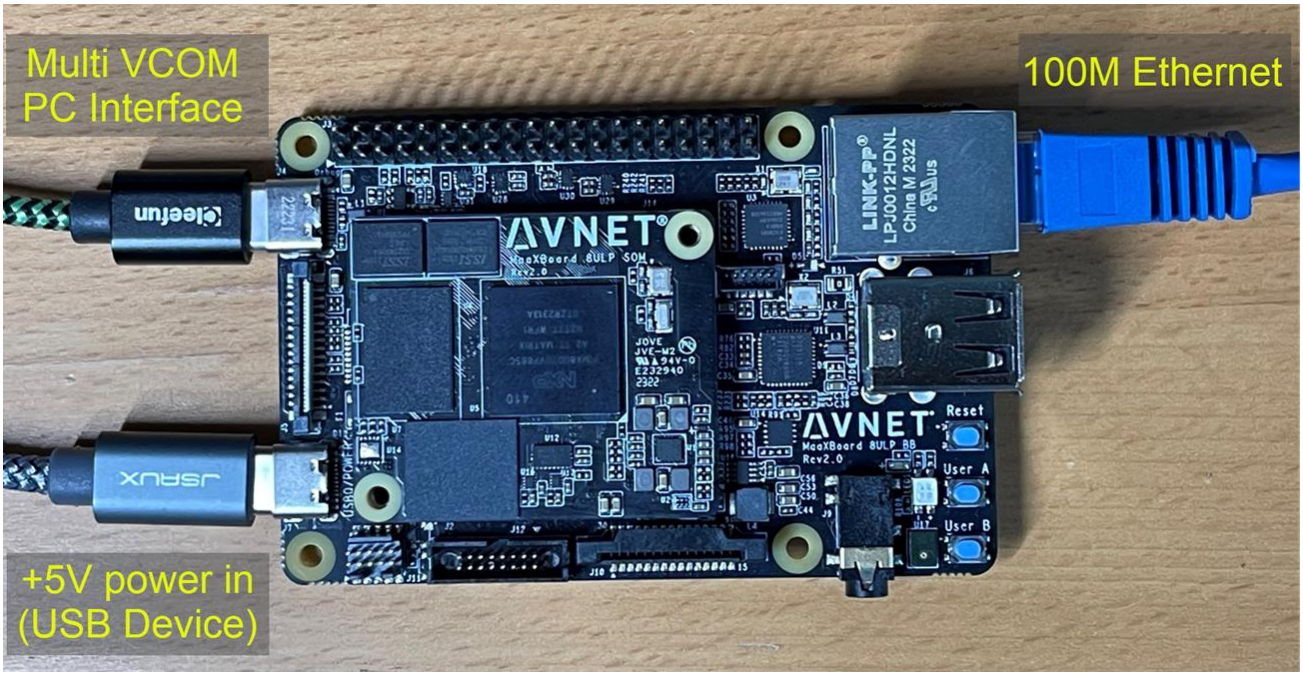
5.3 Important Reference Documents

- MaaXBoard 8ULP QuickStart Card
- MaaXBoard 8ULP Product Brief
- MaaXBoard 8ULP Hardware User Guide *(this document)*
- NXP MIMX8ULPRM Reference Manual

5.4 Hardware Setup for Application Development

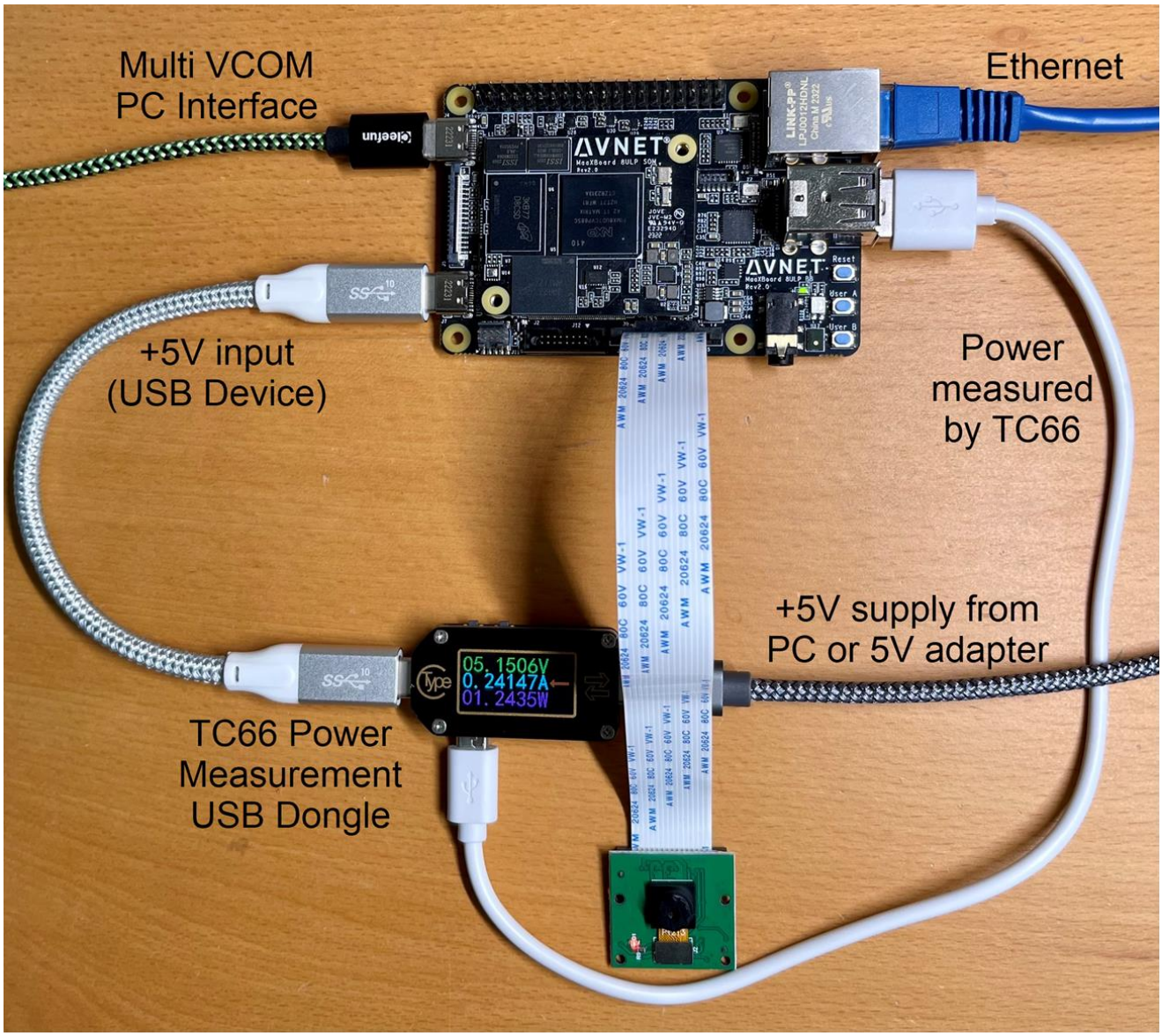
The simplest minimal development setup is shown below

This provides +5V power, console debug interfaces and network connectivity



The development setup below adds:

- 5MP MIPI-CSI camera and
- the ability to read-back current measurements from an external TC66 power measurement USB dongle



To this setup a 7-inch touch panel display can also be added via the MIPI-DSI connector on left side of the board

6 MaaXBoard 8ULP Architecture & Features

6.1 Features

NXP Processor (PIMX8UD7CVP08SC)
2x Arm® Cortex®-A35 @ 800 MHz
1x Arm® Cortex®-M33 @ 216 MHz
1x Cadence® Tensillica® Hifi 4 DSP @475 MHz for advanced audio, voice and ML processing
1x Fusion DSP @200 MHz for low-power voice and sensor hub processing
3D/2D GPU @ 317 MHz (supports Open GL® ES 3.1, OpenCLTM, Vulkan®)
EdgeLock™ security enclave
RISC-V powered Power Management Subsystem (µpower)

NXP PMIC (PCA9460BUKZ)
PCA9460B 13-channel PMIC for Ultra Low Power applications

Memory
2GB LPDDR4X (x32b)
8MB PSRAM
896KB OCRAM
32GB eMMC
4MB QSPI NOR

Camera and Display MIPI Interfaces
1x MIPI DSI (4-lane) with PHY (compatible 7-inch and 5-inch displays available from Avnet)
1x MIPI CSI (2-lane) with PHY (compatible 5MP CSI camera available from Arducam)

USB Host and Device Interfaces
2x USB 2.0 Host ports (type-A)
1x USB 2.0 Device port (type-C)

Network Connectivity
10/100 Ethernet (Microchip KSZ8081RNBCA PHY)
Wi-Fi 5 / BT5.1 wireless M.2 module + U.FL external antenna (optional add-on accessory item)

Audio Resources
Stereo audio codec (DA7212)
Stereo headphone jack
1x digital microphone (MP34DT05)

Expansion Interfaces
Pi-HAT compatible 40-pin header,
MikroE Click 16-pin header
ADC/DAC 6-pin header.

Debug Interfaces
USB-to-serial bridge to three UARTs (A35 #0, A35 #1 and M33 debug console interfaces)
USB to I/O expander for remote control & monitoring (16 signals)
Integrated USB to SWD/JTAG debugger interface
10pin SWD/JTAG header for use with external J-LINK or NXP debug probe

6.2 Block Diagram – NXP i.MX8ULP Processor

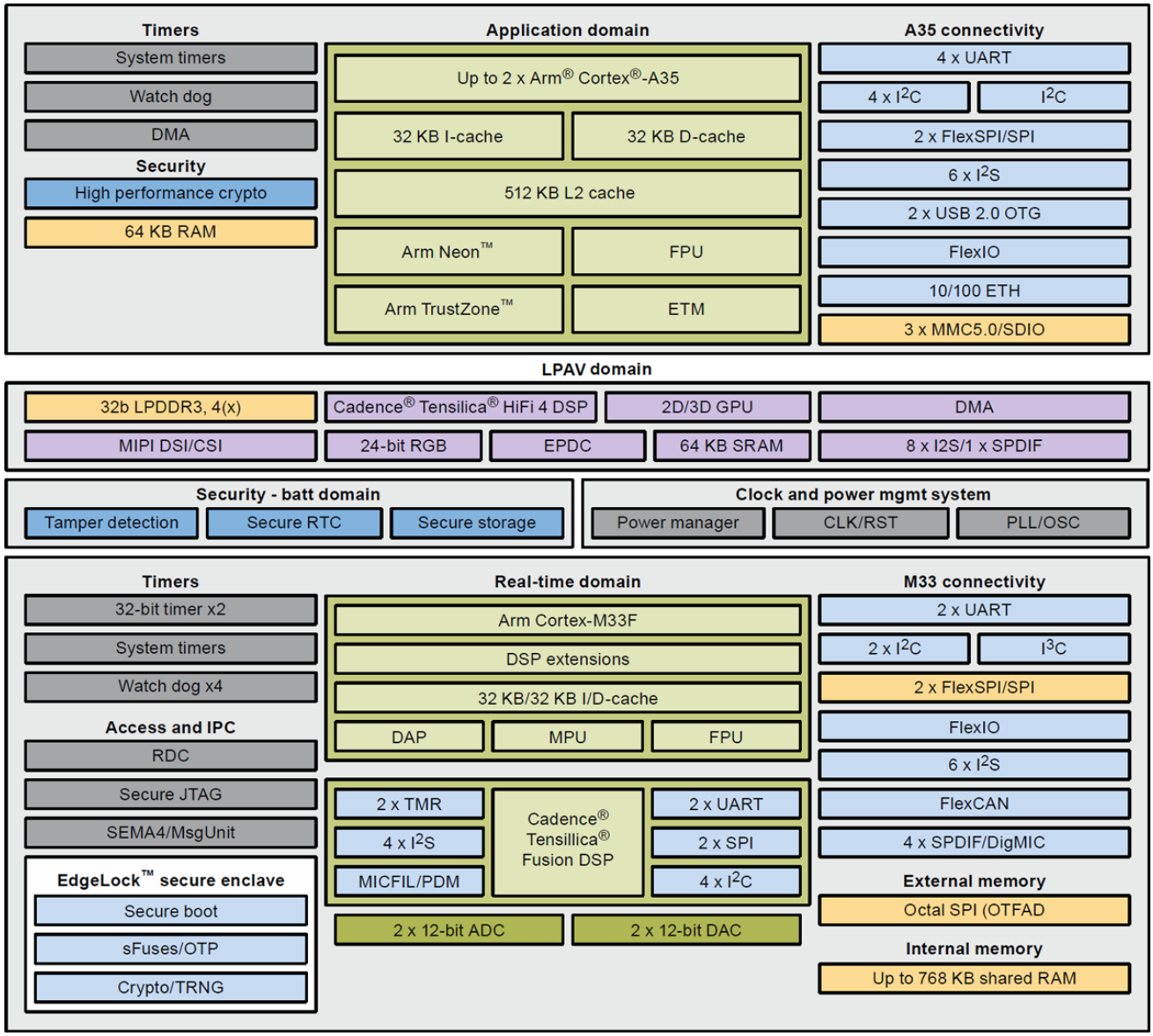
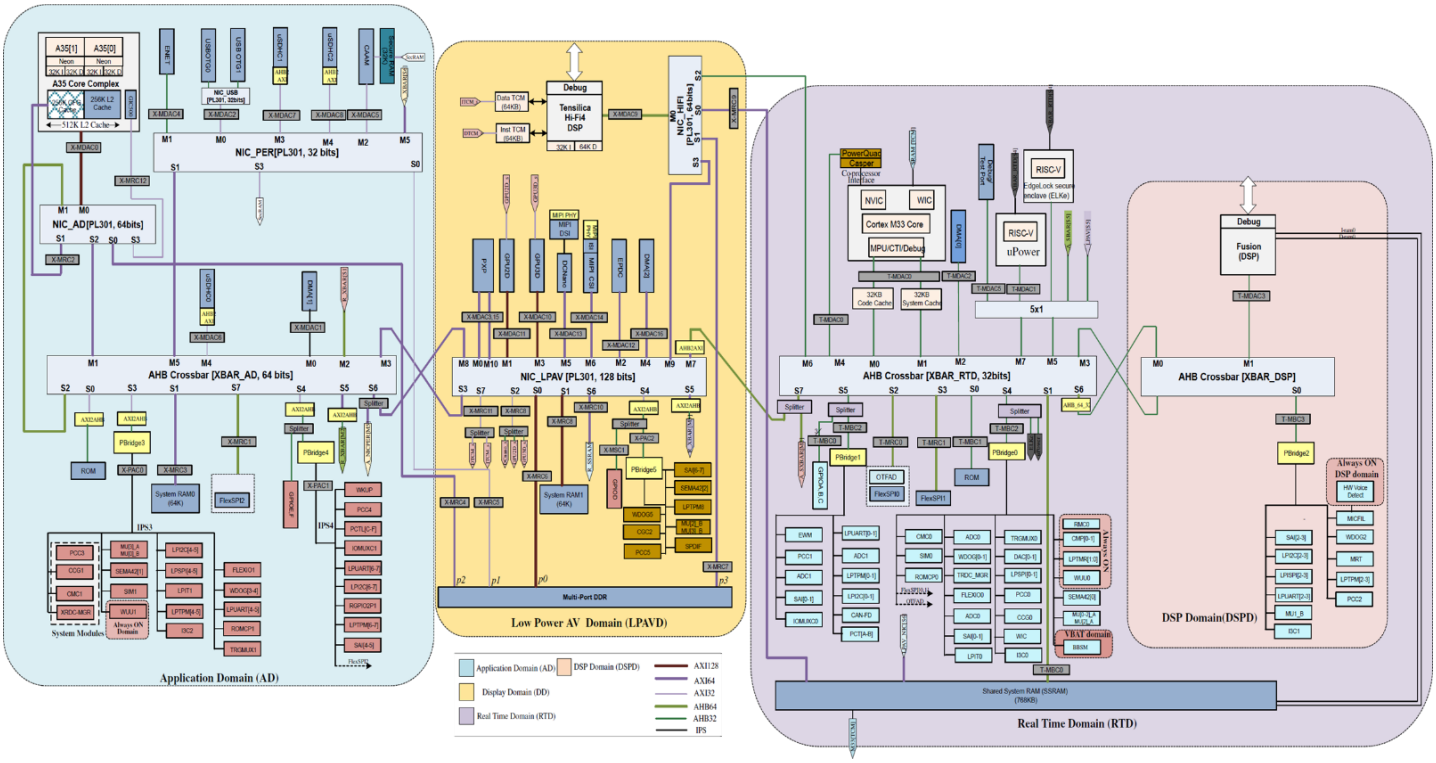


Figure 2 – i.MX 8ULP vs i.MX 8ULP-CS Processor Block Diagram

6.3 8ULP Architecture Diagram



Refer to last page of Chapter 2 (page 36) in the i.MX 8ULP Reference Manual (***IMX8ULPRM_Rev1_DraftA.pdf*** or later) for a higher-resolution version of this 8ULP architecture diagram

6.4 Block Diagram – MaaXBoard 8ULP

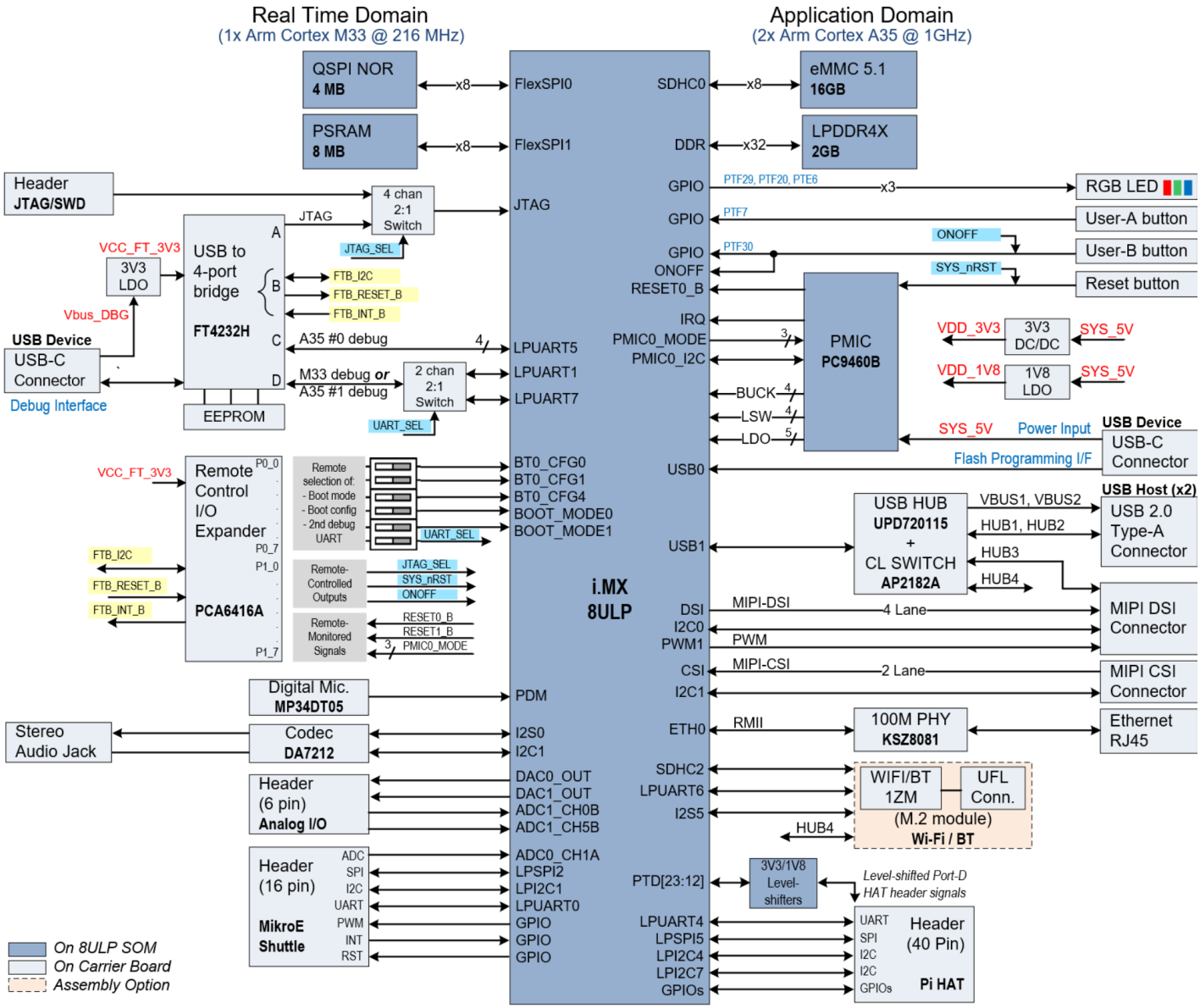
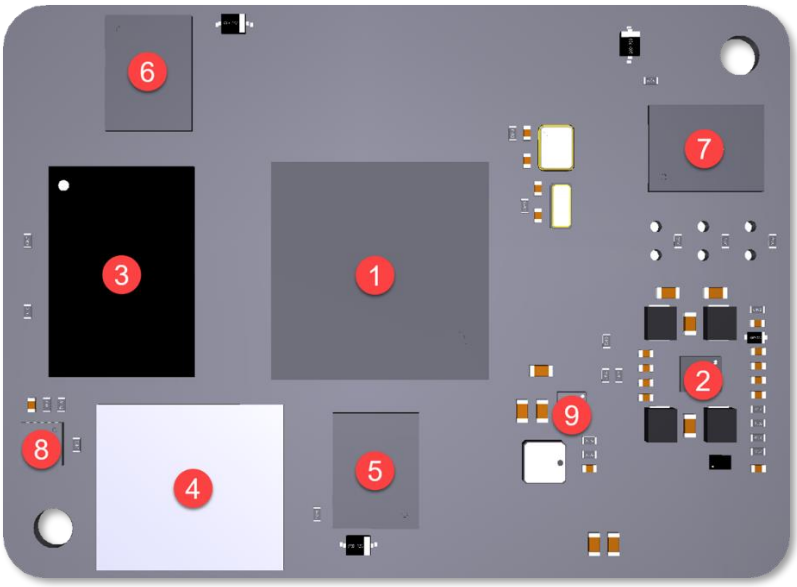


Figure 3 – MaaXBoard 8ULP Block Diagram

Boot Switch configuration

SW5							
8 (MSB)	**7**	**6**	**5**	**4**	**3**	**2**	**1 (LSB)**
BOOT_MODE1	BOOT_MODE0	BT1_CFG14	BT1_CFG13	BT0_CFG4	BT0_CFG3	BT0_CFG1	BT0_CFG0
=X **Boot Type** 00 - Boot From Fuses 01 - Serial Downloader **10 - Internal Boot (Development)** 11 - Reserved	=X	=0 **A35 Boot Type** **00 - uSDHC** 01 - SPI NAND 10 - SPI NOR 11 - Reserved	=0	=X **M33 boot interface** **00 - FlexSPI0 NOR** 01 - FlexSPI0 NAND 10 - uSDHC0 (Partial active mode) 11 - Reserved	=0	=X **Dual Boot** 0 - Boot from eMMC **1 - Boot from A35/eMMC and M33/QSPI**	=X **LP Boot** **0 - No Low Power Boot** 1 - Boot from M33 with A35 on demand

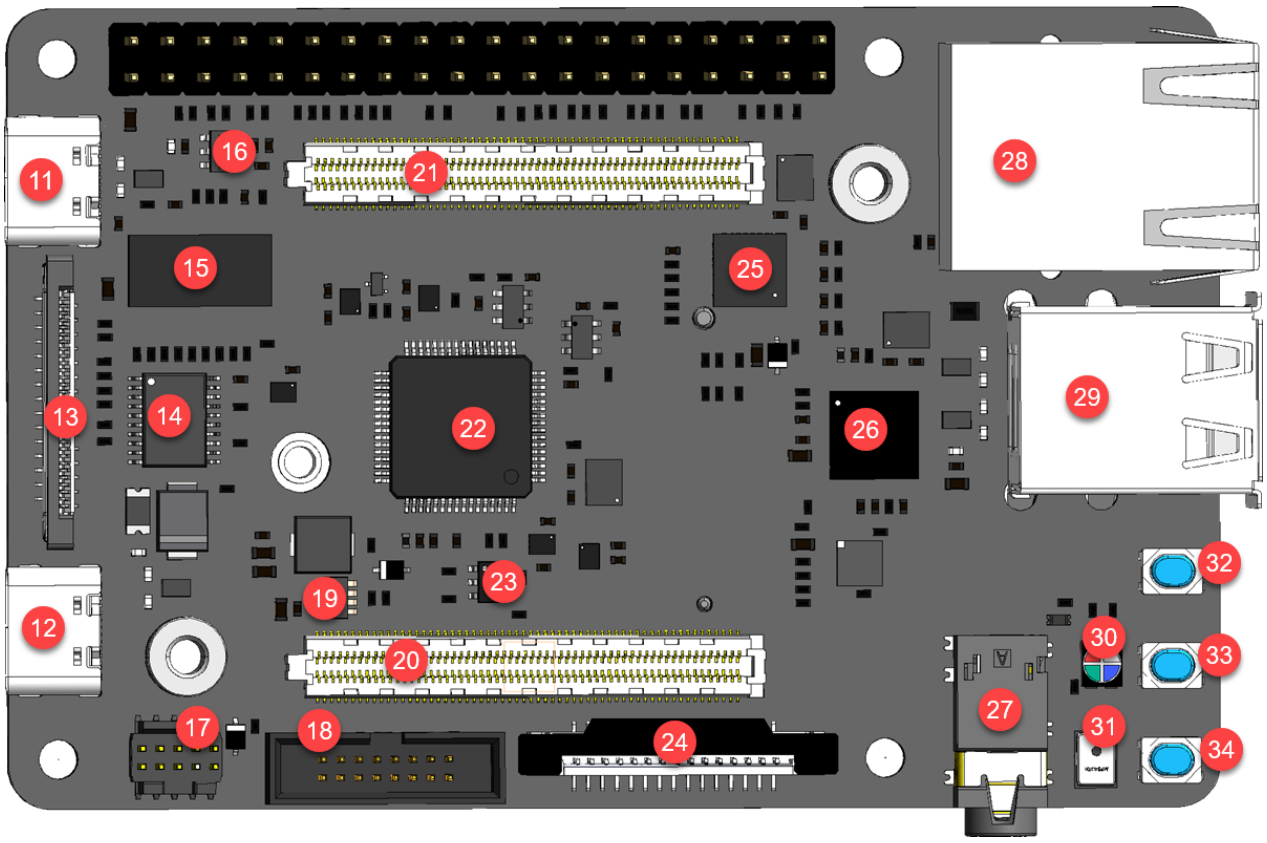
6.5 MaaXBoard 8ULP SOM Component Locations



#	Ref	Component Description	Manufacturer and P/N	Domain
1	U5	NXP iMX 8ULP processor	NXP MIMX8UD7DVP10SA	A35/M33
2	U1	NXP PCA9460B PMIC	NXP PCA9460BUK	n/a
3	U6	LPDDR4X SDRAM memory	Micron MT53E512M32D1ZW-046 IT:B	A35-only
4	U7	eMMC Flash (32GB)	ISSI / Micron EMMC16G-TB29-PZ90	A35/M33
5	U8	Octal SPI NOR HyperFlash	Spansion S26KS256SDPBHI020	A35-only
6	U13	Octal SPI PSRAM	ISSI IS66WVO8M8DALL-200BLI	M33-only
7	U15	Octal SPI NOR Flash	Adesto ATXP032-CCUE-T	M33-only
8	U14	0V6 LDO for LPDDR4X (**NI**)	Renesas (Intersil) ISL80111RAJZ	n/a
9	U28	VDD3V3 dc/dc regulator	Richtek RT8010	n/a
10	U2	Ext. Load Switch (**NI**)	Onsemi NCP451AFCT2G	n/a

Table 3 – Key Components on MaaXBoard 8ULP SOM

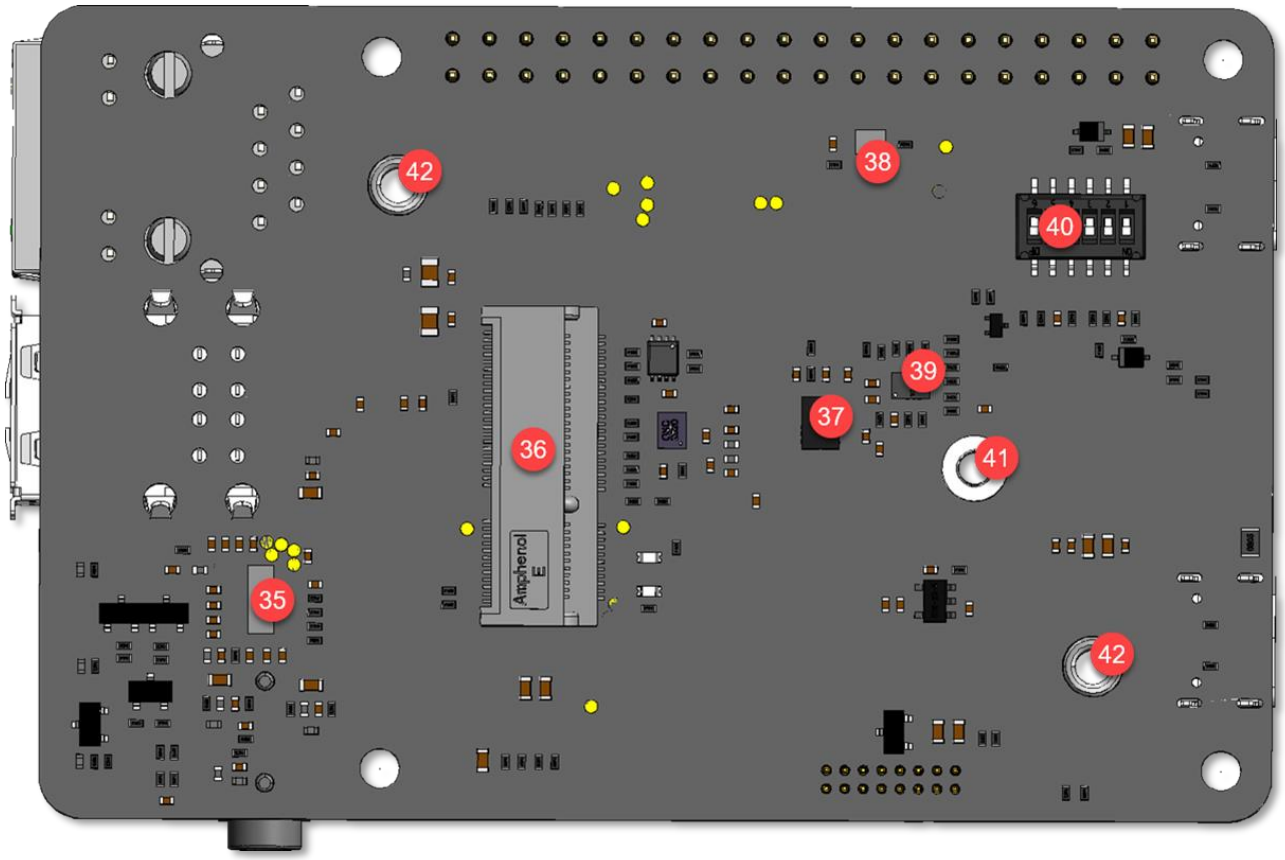
6.6 MaaXBoard 8ULP BaseBoard Component Locations (Top)



#	Ref	Component Description	#	Ref	Component Description
11	J30	USB-C Remote Debug interface	23	U44	EEPROM for FT4232
12	J22	USB-C Download & Power interface	24	J4	MIPI CSI camera Connector
13	J5	MIPI DSI Display connector	25	U24	RMII Ethernet PHY
14	U30	8bit 3-state buffer/driver *(TSSOP48)*	26	U47	4-port USB hub
15	U59	16bit 3-state buffer/driver *(TSSOP20)*	27	J29	Stereo audio Jack
16	U46	3V3 LDO (for FTDI debug interface)	28	J14	Gig Ethernet RJ45 connector
17	J16	JTAG/SWD 10-pin header	29	J26	Stacked USB host connectors
18	J15	MikroE Click Shuttle 16-pin header	30	LED1	RGB LED
19	U19	3V3 dc/dc regulator	31	U1	Digital Microphone
20	J27	SS5 120-pin B2B connector (lower)	32	S1	RESET button
21	J28	SS5 120-pin B2B connector (upper)	33	S2	USER-1 button
22	U37	FT4232H FTDI 4-port USB bridge	34	S3	USER-2 button

Table 4 – Key Components on MaaXBoard 8ULP BaseBoard (top)

6.7 MaaXBoard 8ULP BaseBoard Component Locations (Bottom)



#	Ref	Component Description	#	Ref	Component Description
35	U13	Audio Codec	39	U8	8bit IO expander
36	J10	M.2 Wi-Fi/BT module connector	40	SW3	Boot mode DIP switches
37	U42	JTAG/SWD source selector	41	MH	M.2 module mounting hole
38	U58	Debug UART source selector	42	MH	8ULP SOM mounting holes

Table 5 – Key Components on MaaXBoard 8ULP BaseBoard (bottom)

6.8 Boot DIP-Switches, Button-Switches and LEDs

6.8.1 Boot Mode DIP Switches (SW3)

DIP switches for manual strapping of boot-mode and config settings are on back of the PCB

SW3 #	Signal Name	Selected Function Description	
1	BT_CFG0	0 1	No Low-Power Boot LP boot from M33, boot A35 on demand
2	BT_CFG1	0 1	Boot from eMMC Boot from A35/eMMC and M33/QSPI
3	BT_CFG4	0 1	M33 boot from SPI NOR M33 boot from eMMC
4	BT_MODE0	00 01 10 11	Boot From Fuses Serial Downloader Internal Boot (Development) Reserved
5	BT_ MODE1		
6	JTAG_SEL	0 1	FTDI interface (OpenOCD debugger) 10-pin header (External debugger probe)

6.8.2 Push-Button Switches

Three pushbuttons are located near the board edge, in the bottom-right corner

Ref. Des	Switch Name	Button Switch Function	I.MX 8ULP GPIO Pin	8ULP Board Function
S1	RESET	VDD_3V3 On/Off *(SNVS IN power domain)*	n/a	System Reset, active low
S2	USER-A	WAKEUP *(SNVS ANA power domain)*	PTF7	GPIO Input
S3	USER-B	WAKEUP *(SNVS ANA power domain)*	PTF30	GPIO Input / ONOFF input

6.8.3 Status LEDs

Ref. Des.	LED Status Function	LED Color	I.MX 8ULP GPIO Pin	8ULP Board Function
D15	PWR	Green	n/a	3V3 status
LED1	USER-RED	Red	PTF29	GPIO / PWM
LED1	USER-GREEN	Green	PTF20	GPIO / PWM
LED1	USER-BLUE	Blue	PTE6	GPIO / PWM

6.9 Memory Resources

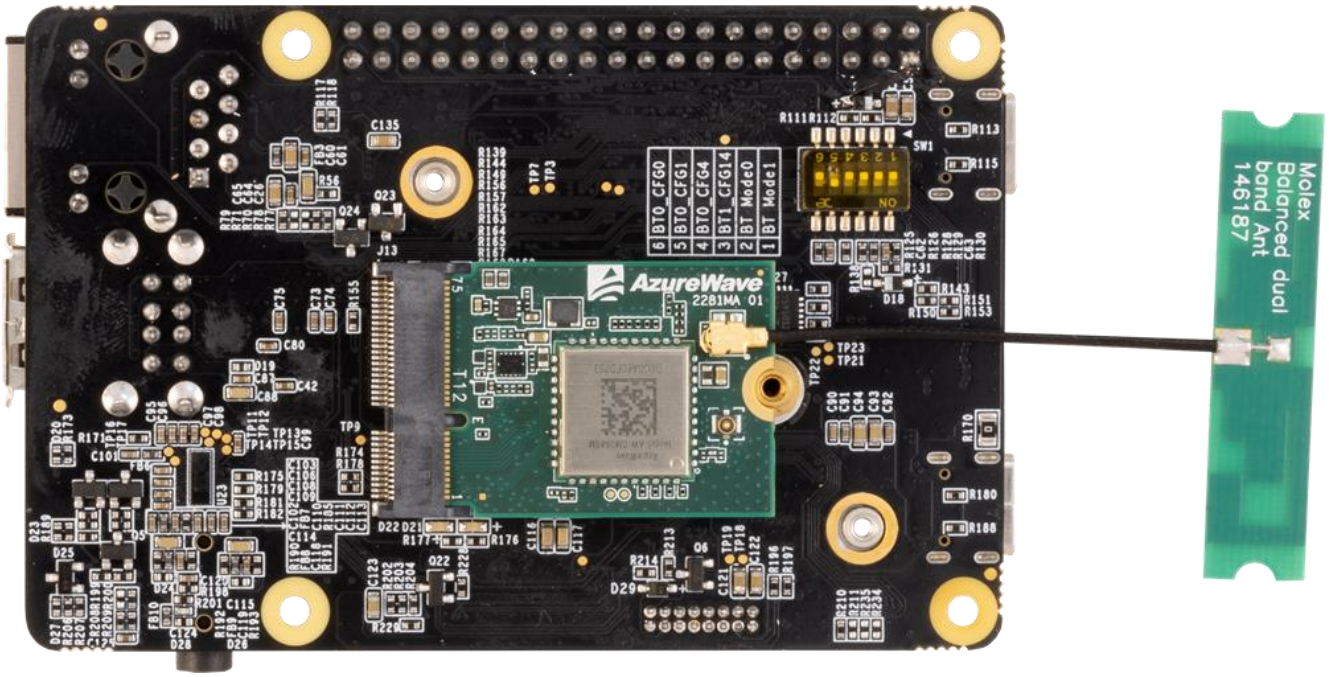
Onboard memory resources are similar to what is available on the NXP MIMX8ULP EVK board (For the application processor however, booting from NOR/NAND SPI flash is not supported)

Memory Interface	MaaXBoard 8ULP SOM	Mem Size	NXP 8ULP-EVK SOM	Mem Size
DDR	LPDDR4X *MT53E512M32D1ZW-046 IT:B*	2 GB	LPDDR4 *MT53D512M32D2DS-053 WT:D*	2 GB
SDHC0	eMMC *EMMC16G-TB29-PZ90*	16 GB	eMMC *SDINBDA6-32G-I*	32 GB
SDHC1	*-not used-*	*n/a*	*-not used-*	*n/a*
SDHC2	(Wi-Fi/BT module)	*n/a*	(Wi-Fi/BT module)	*n/a*
FlexSPI0	M33 Octal SPI NOR Flash *ATXP032-CCUE-T*	4 MB	M33 Octal SPI NOR Flash *ATXP032-CCUE-T*	4 MB
FlexSPI1	M33 Octal SPI PSRAM *IS66WVO8M8DALL-200BLI*	8 MB	M33 Octal SPI PSRAM *APS6408L-OBM-BA*	8 MB
FlexSPI2	*-not used-*	*n/a*	A35 Octal SPI NOR Flash *MX25UW51345GXDI00*	64 MB

Figure 4 –MaaXBoard 8ULP Memory Compared to EVK

Memory Type	Memory Size	8ULP Interface	Avnet Supplier	Part Number
LPDDR4X SDRAM	2 GB	DDR	Micron	MT53E512M32D1ZW-046 IT:B
eMMC flash	32 GB	SDHC0	Micron	MTFC32GAZAQHD-IT
Octal SPI NOR Flash	4 MB	FlexSPI1	Renesas (Adesto)	AT25QL128A-UIUE-T
Octal SPI PSRAM	8 MB	FlexSPI1	ISSI	IS66WVO8M8DALL-200BLI

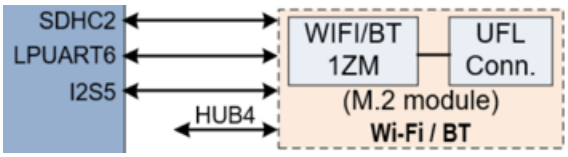
6.10 Wireless Connectivity



MaaXBoard 8ULP uses a **Murata Type-1ZM** Wi-Fi 5 and Bluetooth 5 combo module, which is based on the **NXP 88W8987** device. Both 2.4 GHz and 5 GHz Wi-Fi operation is supported

Interfaces between the NXP 88W8987 based module and the NXP I.MX 8ULP host processor include:

- Wi-Fi SDIO 3.0 (4-bit) interface (uses **SDHC2**)
- BT/BLE UART 4-wire interface (uses **LPUART6**)
- Bluetooth audio PCM interface (uses **I2S5**)
- M.2 USB interface (unused) (uses **HUB4**)



6.10.1 Wi-Fi SDIO Interface

USDHC1 interface is configured for 1.8V operation and is clocked at 200 MHz
(This is the same SDIO interface as used on the i.MX 8ULP-EVK)

6.10.2 BT/BLE UART Interface

LPUART10 including hardware flow is routed from the i.MX 8ULP via a 3.3V to 1.8V level-shifter, to the 1ZM module's Bluetooth UART interface. (Note use of LPUART10 interface is different from what used on the i.MX 8ULP-EVK, which uses LPUART2 for this interface)

6.10.3 BT PCM Audio Interface

SAI1 is routed from from the I.MX 8ULP via a 3.3V to 1.8V level-shifter, to the Murata 1ZM module's Bluetooth UART PCM audio interface. (This use of **SAI1** interface is identical to what is used for this function on the i.MX 8ULP-EVK)

1ZM Module Pin Name	RT Peripheral Resource and Pin# (on MaaXBoard)	NXP i.MX 8ULP-EVK SDK Signal Name	NXP EVK M.2 Signal Name	RT Peripheral Resource and Pin# (on EVK)
BOARD_InitPins	*SAI1*			
BT_PCM_DIN	**SAI1_TXD** [K14]	BT_PCM_TXD	I2S_SD_IN	SAI1_TXD[0] [K14]
BT_PCM_DOUT	**SAI1_RXD** [K13]	BT_PCM_RXD	I2S_SD_OUT	SAI1_RXD[0] [K13]
BT_PCM_CLK	**SAI1_TX_BCLK** [K12]	BT_PCM_BCLK	I2S_SCK	SAI1_TX_BCLK [K12]
BT_PCM_SYNC	**SAI1_TX_SYNC** [J12]	BT_PCM_SYNC	I2S_WS	SAI1_TX_SYNC [J12]

Table 6 – BT PCM Audio Interface (mapped to SDK/EVK signal names)

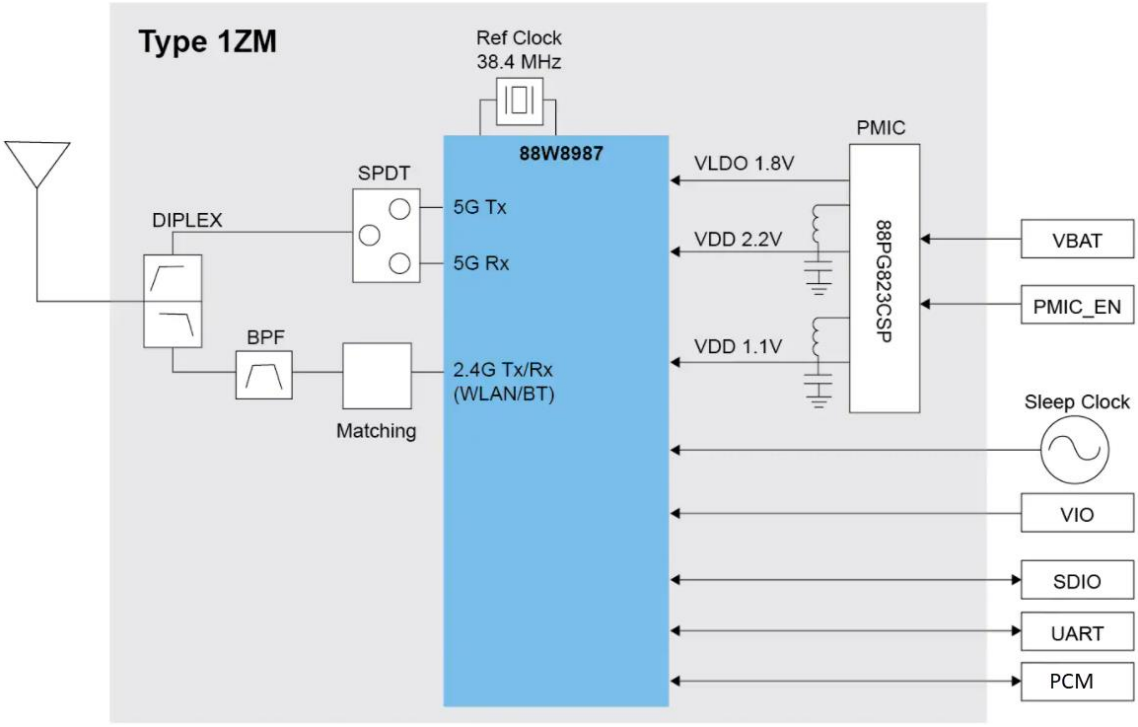


Figure 5 – Murata Type-1ZM Wi-Fi/BT Combo Module Block Diagram

1ZM Module Pin Name	RT Peripheral Resource (on MaaXBoard)	NXP i.MX 8ULP-EVK SDK Signal Name	NXP i.MX 8ULP-EVK M.2 Signal Name	RT Peripheral Resource and Pin# (on EVK)
BOARD_InitUSDHCPins *USDHC1*				
SD_CLK	**SD1_CLK** [D15]	WIFI_SD_CLK	SDIO_CLK	GPIO_SD_B1_01 [D15]
SD_CMD	**SD1_CMD** [B16]	WIFI_SD_CMD	SDIO_CMD	GPIO_SD_B1_00 [B16]
SD_DAT0	**SD1_DATA0** [C15]	WIFI_SD_DAT0	SDIO_DATA0	GPIO_SD_B1_02 [C15]
SD_DAT1	**SD1_DATA1** [B17]	WIFI_SD_DAT1	SDIO_DATA1	GPIO_SD_B1_03 [B17]
SD_DAT2	**SD1_DATA2** [B15]	WIFI_SD_DAT2	SDIO_DATA2	GPIO_SD_B1_04 [B15]
SD_DAT3	**SD1_DATA3** [A16]	WIFI_SD_DAT3	SDIO_DATA3	GPIO_SD_B1_05 [A16]
	n/a	SD_PWREN_B	SD_PWREN_B	GPIO_AD_35 [G17]
	n/a	SD1_CD_B		GPIO_AD_32 [K16]
	n/a	SD1_VSELECT	VSELECT	GPIO_AD_34 [J16]
BOARD_InitM2WifiResetPins				
PMIC_EN (WL_REG_ON)	GPIO_AD_14 *GPIO9_IO13* [N14]	WIFI_RST_B_1V8	/SDIO_RST	GPIO_AD_16 *GPIO9_IO15* [N17]
BOARD_InitUSDHCPins				
	n/a	SD1_VSELECT	VSELECT	GPIO_AD_34 [J16]
BOARD_InitM2UARTPins				
MD_UART_RXD	**LPUART10** [K16]	MD_UART_RXD	UART_RXD	LPUART2 [A6]
MD_UART_TXD	**LPUART10** [H17]	MD_UART_TXD	UART_TXD	LPUART2 [D9]
MD_UART_CTS	**LPUART10** [G17]	MD_UART_CTS	UART_CTS	LPUART2 [B6]
MD_UART_RTS	**LPUART10** [J16]	MD_UART_RTS	UART_RTS	LPUART2 [A5]
UNDEFINED				
	n/a	WIFI_WAKE_B_1V8 WL_HOST_WAKE	/SDIO_WAKE /PERST1	GPIO_AD_29 [M17]
	n/a	BT_WAKE_3V3	/UART_WAKE	GPIO_AD_27 [N16]

Table 7 – Wi-Fi/BT Module Interface

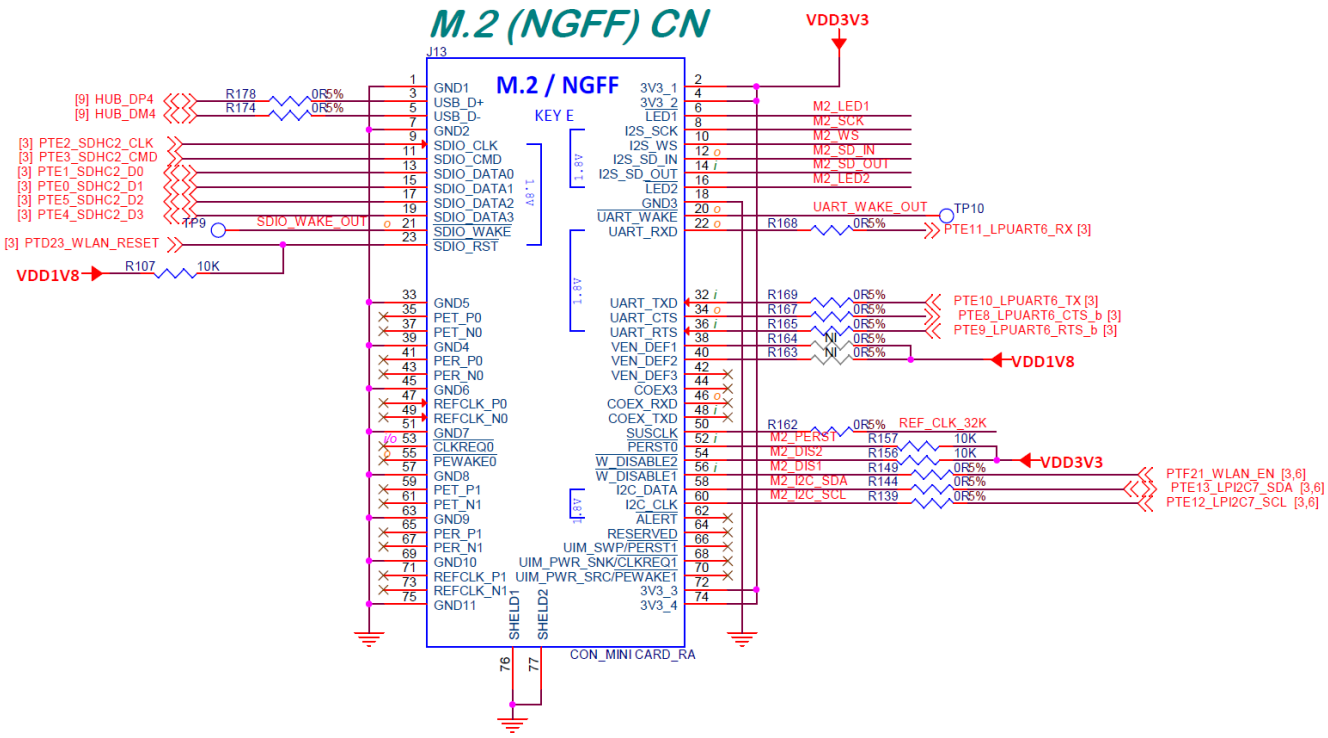
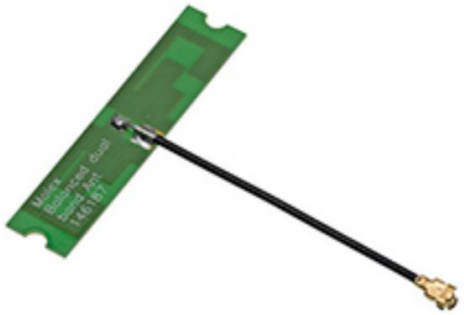


Figure 6 – Detail of Wi-Fi/BT M.2 Module Implementation

6.10.4 Wi-Fi / BT antenna

This board only supports an external antenna, attached via UFL / IPEX MHF connector. The antenna shipped with MaaXBoard 8ULP (as used in regulatory certifications) is Molex p/n: 1461870050



6.11 Peripheral Devices and Interfaces

6.11.1 USB 2.0 FTDI Remote Debug Interface

A subset of the remote-debug interface that is on the NXP 8ULP EVK board, is implemented on MaaXBoard 8ULP. This uses the same FT4232H USB to 4-port serial bridge device, but does not support the power-monitoring controls that are implemented on the NXP EVK.

This FTDI USB supports multiple interfaces:

1) SWD/JTAG debug interface (OpenOCD debugger for the M33)
2) Processor boot mode and boot cfg strapping signals.
3) Remote SYS_RST and ONOFF signals to the processor
4) Remote REMOTE_EN and UART_SEL switch inputs
5) Access to the processor UARTs for system log output
   - A35 #0 core UART
   - A35 #1 core (8ULP) or Pluton UART (8ULP-CS)
   - M33 core UART

For 8ULP-CS the following steps are required to perform RECOVERY reprogram of eMMC

1) User/BCU remotely sets boot cfg and boot mode (ie. via FTDI Port B IO Expander device)
2) User/BCU RESETs the processor into Serial Download mode (via FTDI Port B)
3) ROM code downloads new images from host PC via USB0 and flashes these into eMMC
4) User/BCU remotely restores cfg and boot mode back to the setting for boot from eMMC
5) User/BCU RESETs the processor into normal eMMC boot mode

6.11.2 USB 2.0 Device Interface

USB0 controller is assigned as a **USB Device** interface, implemented with a USB-C connector

6.11.3 USB 2.0 Host Interface

USB1 controller is assigned as a **USB Hub** interface, which supports 4 USB Host interfaces:

- Two stacked USB type-A connectors (eg. for keyboard and mouse)
- USB interface with the M.2 connector (unused for Wi-Fi/BT M.2 modules)
- USB interface with the MIPI display connector (unused for MaaXBoard 7” panel)

6.11.4 10/100 Ethernet (with IEEE 1588 time-sync.)

The 10/100 Ethernet subsystem is comprised of:

- **ENET** i.MX 8ULP Ethernet MAC peripheral,
- Microchip KSZ8081RNBCA Ethernet transceiver (U24) with RMII interface,
- RJ45 (J14) with integrated magnetics.

6.11.5 CAN-FD

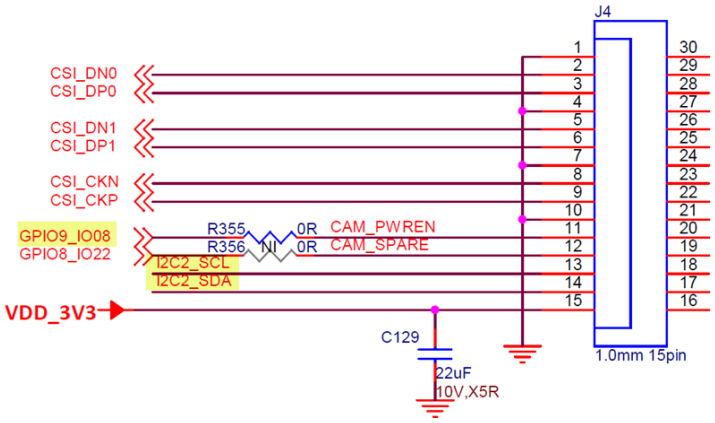
CAN0 TXD and RXD signals are **not** available (signals are not pinned-out from the SOM)

6.11.6 MIPI-DSI Display and Touchscreen

2-lane, supports up to 1280x720 display. This has same 30-pin MIPI connector form-factor as on Raspberry Pi but has customized pinout and includes I2C touchscreen controller interface

6.11.7 MIPI-CSI Camera

The 2-lane, 15-pin MIPI connector pinout is the same as what is used on Raspberry-Pi board



Camera Control I/O	Processor I/O
CAM_PWREN	GPIO09_IO08
CAM_I2C_SCL	I2C2_SCL
CAM_I2C_SDA	I2C2_SCL

Note: The 5 MP MIPI-CSI MaaXBoard camera (add-on option) is based on the same OV5640 image sensor as used with the NXP i.MX 8ULP-EVK board.

6.11.8 Digital Microphones

A single onboard PDM digital microphone is supported (ST p/n: MP34DT05-A). This is located between the stereo audio jack and the button switches (in bottom-right corner of the PCB). This drives the following input to the 8ULP processor:

PDM Microphones	PDM Data Input
MIC0	PDM_DATA_0

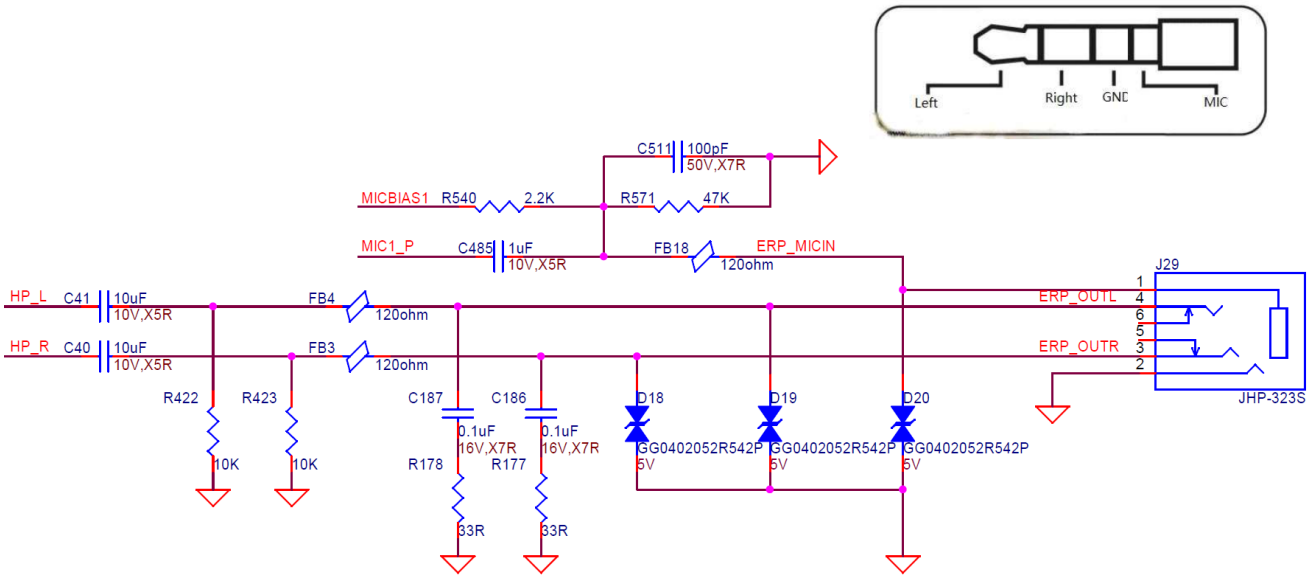
6.11.9 Audio Codec

SAI2 interface of i.MX 8ULP (Serial Audio Interface #2) is connected to the NXP SGTL5000 stereo audio Codec. PCM audio between Wi-Fi/BT module and the Codec, requires routing through the i.MX 8ULP processor.

Note! Use of SAI2 and a different Codec means that implementation of audio applications is different to that of the SDK examples targeting the i.MX 8ULP EVK.
(Refer to Ref.Design #1 for guidance)

SAI1 (Serial Audio Interface #1) connects the i.MX 8ULP processor with the Bluetooth PCM audio interface of the WiFi/BT module.

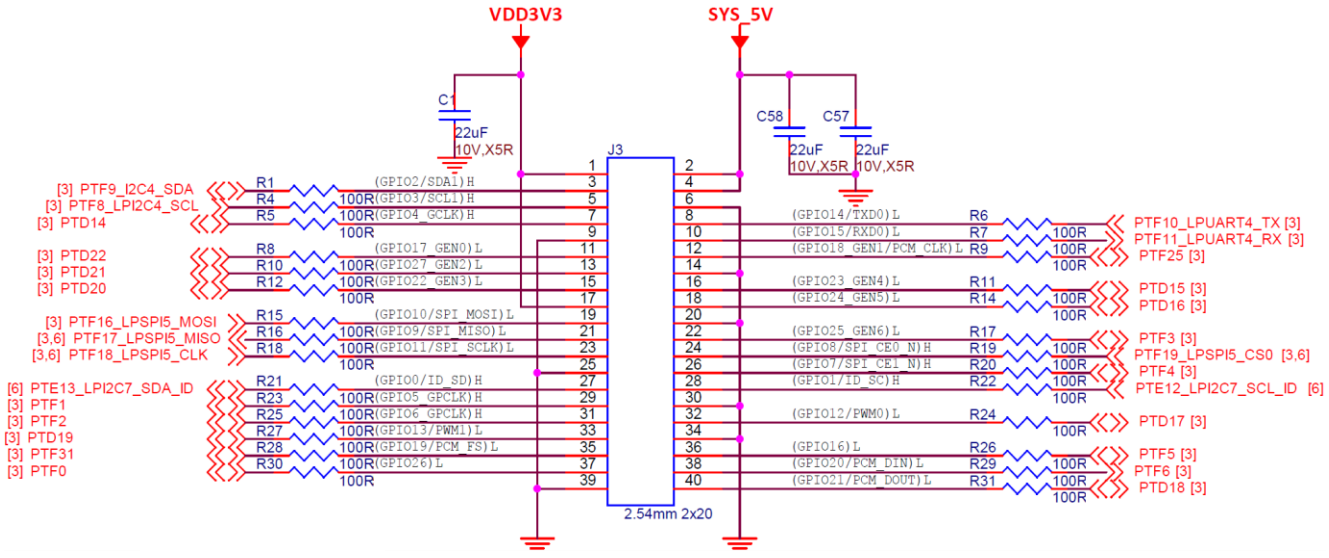
6.11.10 J9: Stereo Audio Jack



6.11.11 J1: Pi-HAT compatible 40-pin header

Pin #	A35 M33	Possible HAT Pin Function	MaaXBoard 8ULP Signal Name	Pin #	A35 M33	Possible HAT Pin Function	MaaXBoard 8ULP Signal Name
1	-	3V3	VDD_3V3	2	-	5V	5V_SYS
3	A35	I2C_SDA	LPI2C4_SDA	4	-	5V	5V_SYS
5	A35	I2C_SCL	LPI2C4_SCL	6	-	GND	GND
7	A35	GPIO / GPCLK0	PTD14	8	A35	UART_TX	PTF10_LPUART4_TX
9	-	GND	GND	10	A35	UART_RX	PTF11_LPUART4_RX
11	A35	GPIO / RTS	PTD22	12	A35	PCM_CLK	PTF25
13	A35	GPIO	PTD21	14	-	GND	GND
15	A35	GPIO	PTD20	16	A35	GPIO	PTD15
17	-	3V3	VDD_3V3	18	A35	GPIO	PTD16
19	A35	SPI_MOSI	PTF16_LPSPI5_MOSI	20	-	GND	GND
21	A35	SPI_MISO	PTF17_LPSPI5_MISO	22		GPIO	PTF3
23	A35	SPI_SCLK	PTF18_LPSPI5_CLK	24	A35	SPI_CS0	PTF19_LPSPI5_CS0
25	-	GND	GND	26	A35	SPI_CS1	PTF4
27	A35	EEPROM_SDA	PTE13_LPI2C7_SDA_ID	28	A35	EEPROM_SCL	PTE12_LPI2C7_SCL_ID
29	A35	GPIO / GPCLK1	PTF1	30	-	GND	GND
31	A35	GPIO / GPCLK2	PTF2	32	A35	GPIO / PWM0	PTD17
33	A35	GPIO / PWM1	PTD19	34	-	GND	GND
35	A35	GPIO / PCM_FS	PTF31	36	A35	GPIO / CTS	PTF5
37	A35	GPIO	PTF0	38	A35	GPIO / PCM_DIN	PTF6
39	-	GND	GND	40	A35	GPIO / PCM_DOUT	PTD18

Table 8 – Pi-HAT compatible 40-pin header (J1)



Note: Refer to the following webpage for Raspberry Pi HAT compatibility: *https://pinout.xyz/pinout/*

6.11.12 MikroE Click Boards

- Over 1100+ Click Boards available (orderable from Avnet)
- Inexpensive Pi HAT adapters available (these support 2 Click boards)
- Parametric search tool on MikroE website
- Open source library code available at https://www.mikroe.com/click-boards

6.11.13 MikroE Pi-2-Click HAT Adapter Pinout

- Pinout for this HAT adapter ($8.00) is shown below (accommodates two Click boards)

Pin #	Pi-2-Click HAT Pin Function	MaaXBoard 8ULP Signal Name	Pin #	Pi-2-Click HAT Pin Function	MaaXBoard 8ULP Signal Name
1	**3V3**	**VDD_3V3**	2	**5V**	**5V_SYS**
3	GPIO2 ***SDA***	LPI2C4_SDA	4	**5V**	**5V_SYS**
5	GPIO3 ***SCL***	LPI2C4_SCL	6	**GND**	**GND**
7	GPIO4 ***AN1***	PTD14	8	GPIO14 ***UART_TX***	PTF10_LPUART4_TX
9	**GND**	**GND**	10	GPIO15 ***UART_RX***	PTF11_LPUART4_RX
11	GPIO17 ***PWM2***	PTD22	12	GPIO18 ***PWM1***	PTF25
13	GPIO27 *nc*	PTD21	14	**GND**	**GND**
15	GPIO22 *nc*	PTD20	16	GPIO23 *nc*	PTD15
17	**3V3**	**VDD_3V3**	18	GPIO24 *nc*	PTD16
19	GPIO10 ***SPI_MOSI***	PTF16_LPSPI5_MOSI	20	**GND**	**GND**
21	GPIO9 ***SPI_MISO***	PTF17_LPSPI5_MISO	22	GPIO25 *nc*	PTF3
23	GPIO11 ***SPI_SCLK***	PTF18_LPSPI5_CLK	24	GPIO8 ***SPI_CS0***	PTF19_LPSPI5_CS0
25	**GND**	**GND**	26	GPIO7 ***SPI_CS1***	PTF4
27	ID_SDA *nc*	PTE13_LPI2C7_SDA_ID	28	ID_SCL *nc*	PTE12_LPI2C7_SCL_ID
29	GPIO5 ***RST1***	PTF1	30	**GND**	**GND**
31	GPIO6 ***INT1***	PTF2	32	GPIO12 *nc*	PTD17
33	GPIO13 ***AN2***	PTD19	34	**GND**	**GND**
35	GPIO19 ***RST2***	PTF31	36	GPIO16 *nc*	PTF5
37	GPIO26 ***INT2***	PTF0	38	GPIO20 *nc*	PTF6
39	**GND**	**GND**	40	GPIO21 *nc*	PTD18

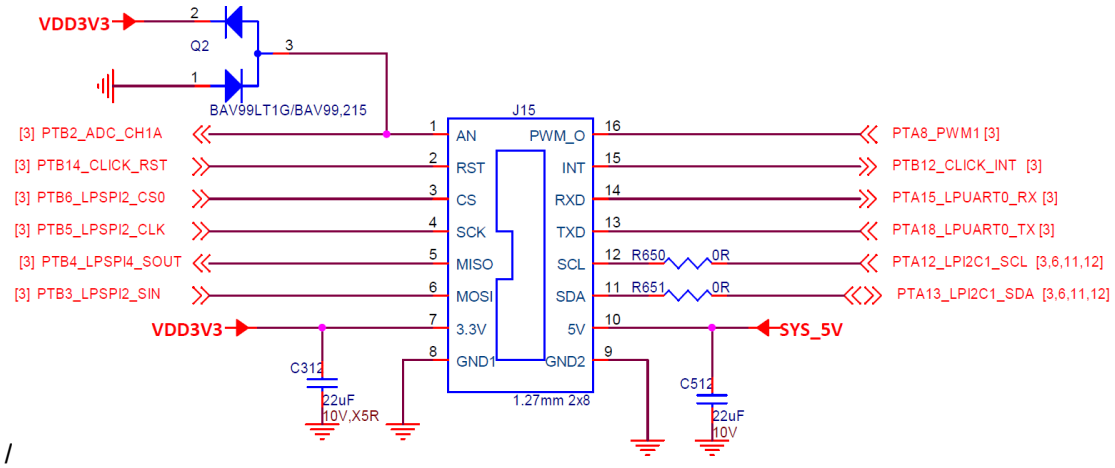
6.11.14 J15: 16-pin MikroE Click Shuttle expansion header

Pin #	MikroE Click Function	MaaXBoard 8ULP Signal Name	Pin #	MikroE Click Function	MaaXBoard 8ULP Signal Name
1	AN	PTB2_ADC_CH1A	2	PWM	PTA8_PWM1
3	RST	PTB14_CLICK_RST	4	INT	PTB12_CLICK_INT
5	CS	PTB6_LPSPI2_CS0	6	RXD	PTA15_LPUART0_RX
7	SCK	PTB5_LPSPI2_CLK	8	TXD	PTA18_LPUART0_TX
9	MISO	PTB4_LPSPI4_SOUT	10	SCL	PTA12_LPI2C1_SCL
11	MOSI	PTB3_LPSPI2_SIN	12	SDA	PTA13_LPI2C1_SDA
13	3V3	VDD3V3	14	5V	SYS_5V
15	GND	GND	16	GND	GND

Table 9 – 16-pin MikroE Click Shuttle expansion header (J15)

Notes:

1) **All** MikroE Click I/Os are directly connected to M33 peripherals or M33 GPIOs



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6.11.15 Pi HAT Expansion Boards

- A strong ecosystem of Pi HAT boards support a wide range of functionality
- See listings at websites such as https://pinout.xyz/boards
- Height of stacked boards is minimized as i.MX 8ULP does not require heatsink

6.11.16 SWD/JTAG debugger 10-pin mini-header

- The 10-pin Mini-header by default supports the SWD interface tabled below

JTAG	MCU-LINK SWD	Pin #	Pin #	MCU-LINK SWD	JTAG
JTAG_TMS	SWD_IO	**2**	**1**	IF_VREF	VDD_3V3
JTAG_TCK	SWCLK	**4**	**3**	GND	GND
JTAG_TDO	SWO	**6**	**5**	GND	GND
JTAG_TDI	IF_TDI	**8**	**7**	IF_ISPEN	*GND**
nRST	IF_RST	**10**	**9**	IF_DETECT	*JTAG_nTRST**

Table 10 – SWD/JTAG debugger 10-pin mini-header (J16)

***Note**: *For JTAG interface: Reconfigure pin 7 and pin 9 PCB bridges to support these signals*

6.12 Power Input, Protection and Regulation

6.12.1 USB type-C Connector

The USB type-C connector is used for 5V power *and* provides a USB-Device interface

6.12.2 ESD Protection

All USB connectors have high-speed ESD protection on their power rails and data lines

6.12.3 Power Regulation

A 5V to 3.3V dc/dc buck convertor regulates the Vcc rail voltage (rated @ 3A max)

6.12.4 Measuring Power Consumption

An inexpensive current-measurement USB power-measurement dongle is recommended during development, in-line with the USB connection to the host computer, for monitoring 5V input current draw. The USB dongle meter shown here can accommodate a type-C or type-A cable connections and is available online for around $20
https://www.amazon.com/Tester-Eversame-Voltmeter-Ammeter-Braided/dp/B07MGQZHGM

Note: An invalid current measurement will be seen if MaaXBoard 8ULP is powered from a USB port from the same PC as the debugger probe!

To achieve a useful current measurement, the board must be powered from a separate power-adapter, or the debugger probe must be fully disconnected.

Figure 7 – Example Current-measurement USB Dongle

6.12.5 8ULP Power Domains

The i.MX 8ULP processor supports multiple power domains as tabled below and detailed on the next page

Power domain	Components
Real-time processor domain (RTD)	Arm Cortex-M33 platform Fusion F1 DSP Security subsystem Power management Multiple peripherals System-level components Three GPIO ports: A, B, and C
Application processor domain (APD)	One or two Arm Cortex-A35 core platform Multiple peripherals Three GPIO ports: D, E, and F
Low-power audio/video domain (LPAV)	HÍFÍ4DSP Graphics Processing Unit 3D (GPU3D) Graphics Processing Unit 2D (GPU2D) LPDDR3/LPDDR4/LPDDR4X interface MIPI-DSI interface MIPI-CSI interface
DGO (always-ON) domain	Reset and system mode control logic Low-leakage Wake-Up Unit (WUU) Analog comparators Low-power timers
VBAT domain	Real-time clock (RTC) Battery-Backed Security Module (BBSM) Battery-Backed Non-Secure Module (BBNSM)

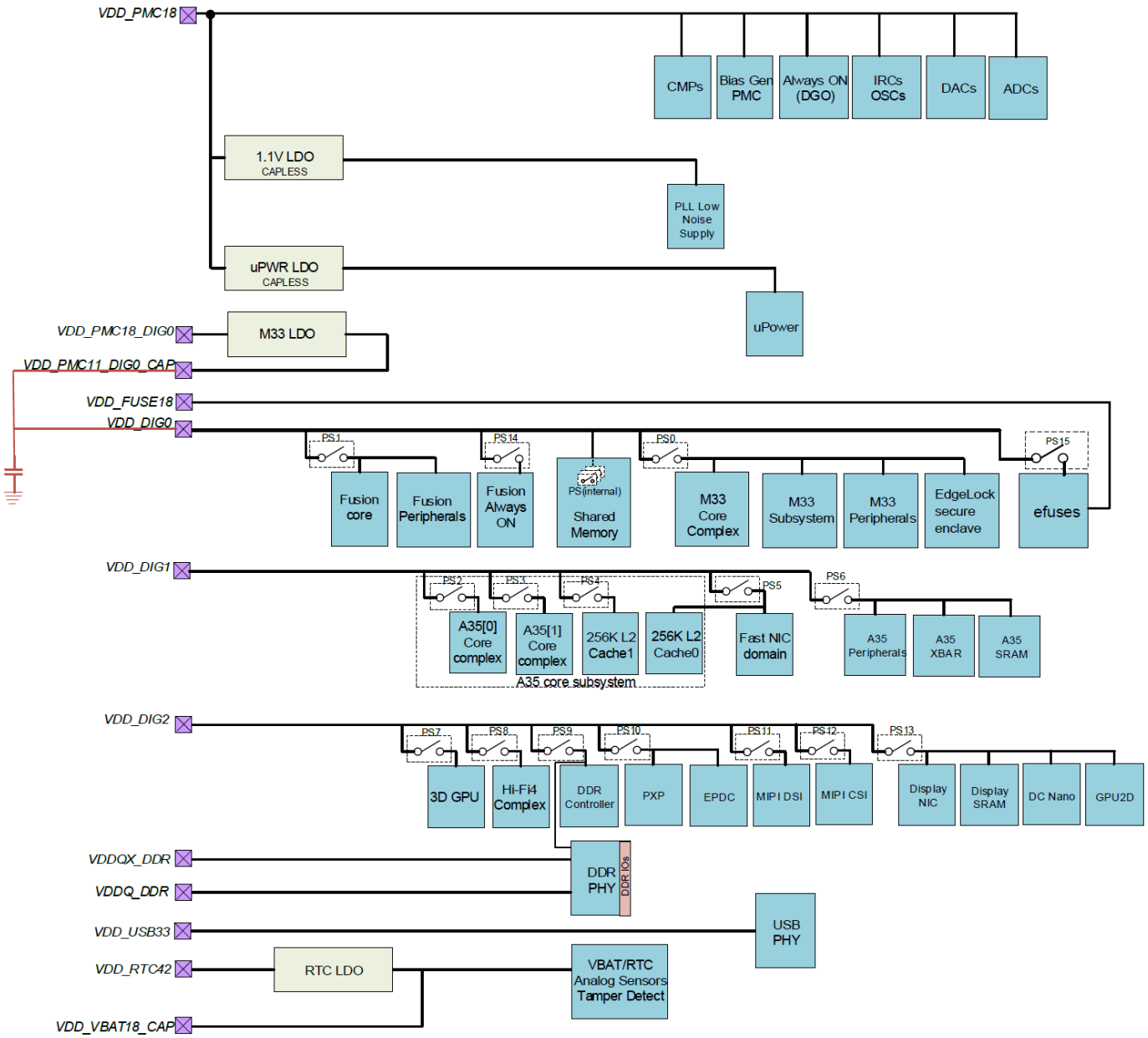


Figure 8 – 8ULP Power Management Scheme

(Refer to Chapter 10, page 820 of the NXP reference manual for the high-resolution diagram)
Testpoints are provided on the SOM for current measurement of three independent power domains: VDD_DIG0, VDD_DIG1 and VDD_DIG2 (requires use of external test instrument).

Software Enablement

At time of publishing this document, the following new factory-programmed Linux BSP image was in use:
maaxboard8ulp-lf-6.1.22-2.0.0-mickledore-20230922-factory

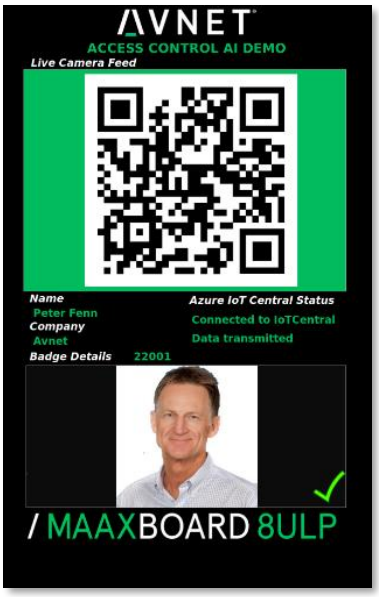
Public links in context of previous version (*MaaXBoard-8ULP_lf-6.1.1-1.0.0_Yocto_20230630*) are tabled below:

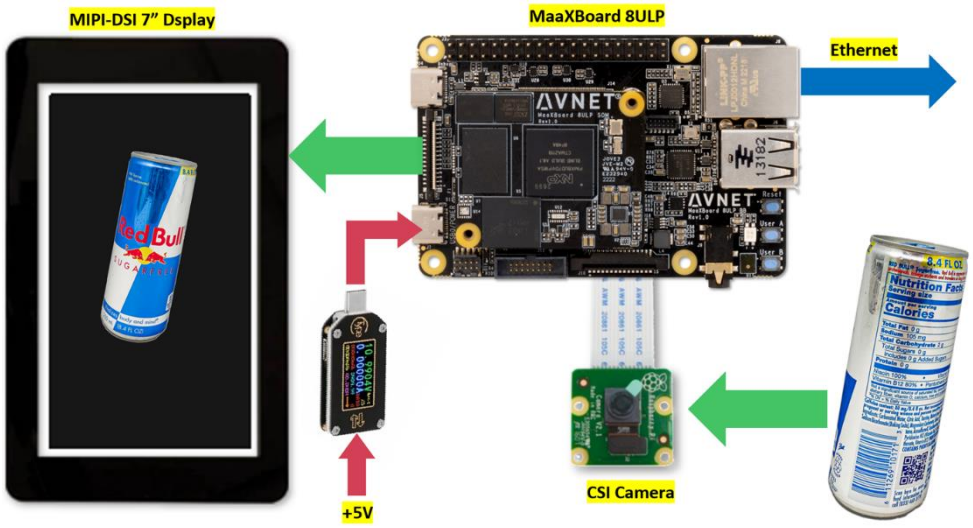
Resource Description	**Links to Avnet Repos**
Pre-built Bootloader image Pre-built Linux BSP image Linux BSP manifest file	u-boot-maaxboard-8ulp.imx avnet-image-full-maaxboard-8ulp-20230620082521.rootfs.wic avnet-image-full-maaxboard-8ulp-20230620082521.rootfs.manifest
Yocto SDK	fsl-imx-wayland-lite-glibc-x86_64-avnet-image-full-armv8a-maaxboard-8ulp-toolchain-6.1-langdale.sh
Yocto source code U-boot source code Linux kernel source code imx-mkimage source code imx-atf source code	https://github.com/Avnet/meta-maaxboard https://github.com/Avnet/uboot-imx.git https://github.com/Avnet/linux-imx.git https://github.com/Avnet/imx-mkimage.git https://github.com/Avnet/imx-atf.git
Release Note Linux Development Guide Linux User Manual	.md doc.pdf doc .md doc.pdf doc .md doc.pdf doc
SDK_2_14_1_EVK-MIMX8ULP	https://mcuxpresso.nxp.com/

7 MaaXBoard 8ULP Example Applications

7.1 Avnet-Supplied Reference Designs

#	Application Name	Key Board Functions Exercised	Repo / Location
1	*Ref.Design #1*: Webserver Out of Box Demo	Webserver, Ethernet, MIPI camera, MIPI display, power modes and power measurement	
2	*Ref.Design #2*: Access Control AI Demo	Ethernet, MIPI camera, MIPI display	
3	*Ref.Design #3:* UPC Food Label Scan Demo	Webserver, Ethernet, MIPI camera, MIPI display	





8 Known Issues

The following should be noted when working with the Rev.3 version production MaaXBoard 8ULP

#	Description of Issue	Comment / Workaround
1	No known issues at this time	

9 Cautionary Notes

ESD - Handling precautions for ESD-vulnerable electronic equipment are strongly recommended. It is advised to touch the metal housing of Ethernet or USB connectors, prior to touching any other part of the PCB.

Connectors - Use care when inserting/unplugging cables, especially with USB-C and audio jack connectors. Finger-support is advised to brace surface mount connectors against excessive lateral force.

MIPI Connectors - The locking mechanism of MIPI-DSI and MIPI-CSI ribbon cable connectors are relatively fragile and should be handled with care. Make sure of alignment and use minimal force when locking.

OTP eFuses – For security reasons, the on-chip OTP fuses in the i.MX 8ULP are one-time programmable. During application development, there should never be a need to program these fuses. Two boot modes are supported via selection jumper (J19). Programming of OTP eFuses will only be necessary when deploying this board in an end-product. It is the user's responsibility to be absolutely certain of their requirements before OTP programming and to not program the fuses by accident.

Note that Avnet accepts no liability and will not replace boards that have been:

- Damaged by ESD or mishandling.
- Compromised through OTP eFuse programming

10 Technical Support

10.1 NXP-hosted Technical Support Resources

The NXP Community Technical Support Forums should be used for questions specific to the i.MX 8ULP processor: https://community.nxp.com/t5/i-MX-Processors/bd-p/imx-processors

NXP also provide a wealth of online i.MX training and App Note resources, accessible from this page: https://www.nxp.com/design/training:TRAINING-EVENTS

10.2 Avnet-hosted Technical Support Resources

Avnet documents & reference designs are available for download from MaaXBoard 8ULP product page: http://avnet.me/MaaXBoard 8ULP

Avnet instructional tutorial blogs will also be linked to from: http://avnet.me/MaaXBoard 8ULP

Avnet technical forum support is available at: http://avnet.me/AvnetBoards_Support

11 Sales Contact Info

For further info on Avnet-designed Starter Kits, contact your local Avnet representative at:

Region	Organization	Contact Webpage	Address & Phone
North America	Avnet Americas	www.avnet.com/contact	2211 South 47th Street Phoenix, AZ 85034, USA Phone: +1-800-585-1602
EMEA	Avnet Silica	avnet-silica.com/contact	Gruber Str. 60c 85586 Poing, Germany Phone: +49-8121-77702
EMEA	EBV	ebv.com/contact	Im Technologypark 2-8 85586 Poing, Germany Phone: +49-8121-774 - 0

12 Disclaimer

MaaXBoard 8ULP is engineered for use as a development board (to facilitate product evaluation and system-level prototyping) as well as for use as a sub-assembly in custom OEM end-products.

Avnet assumes no liability for modifications that a user chooses to make to MaaXBoard 8ULP.

13 Safety Warnings

Safety Warnings

1) It is recommended that this product only be powered via the on board USB type-C connector, from one of the following power sources:

   a) +5V via USB type-C cable, connected to the development computer

   b) +5V via USB type-C cable, connected with a battery of suitable rating

   c) +5V via USB type-C cable, connected to an external +5V, 1A DC power adaptor (a higher rating may be needed if an expansion Pi_HAT or custom board is fitted)

      The external power supply shall comply with relevant regulations and standards applicable in the country of intended use.

2) Only compatible plug-in modules shall be connected to MaaXBoard 8ULP.

   Connection of incompatible devices may affect compliance or result in damage to the unit and void the warranty.

3) This product must be operated in a well-ventilated environment.
   If an enclosure is used, this must provide adequate ventilation.

4) Do not insert or remove any expansion board or cable, without first unplugging the relevant +5V DC power source

5) Ambient operating temperature when using MaaXBoard 8ULP shall not exceed the range of:
   -30C to +85C

14 MaaXBoard 8ULP Accessories

14.1 MIPI DSI 7-inch Capacitive Touch LCD Display *(optional)*

- Supports up to 800 x 1280 resolution
- Compatible with all MaaXBoard SBC platforms.
- Connects to host via a 4-lane MIPI-DSI interface
- Capacitive multi-touch display overlay
- Custom displays available via Avnet Embedded

Part# (and link): AES-ACC-MAAX-DISP2 (MSRP = $105.00)

14.2 MIPI DSI 5-inch Capacitive Touch LCD Display *(optional)*

- Supports up to 720 x 1280 resolution
- Compatible with all MaaXBoard SBC platforms.
- Connects to host via a 4-lane MIPI-DSI interface
- Capacitive multi-touch display overlay
- Custom displays available via Avnet Embedded

Part# (and link): AES-ACC-DISP-5INCH (MSRP = call for more information)

***** Coming Soon *****

14.3 MIPI CSI 5 MP Camera *(optional)*

- High quality 5 MP image sensor
- Compatible with all MaaXBoard SBCs and Raspberry Pi
- Attaches to host via 2-lane MIPI CSI ribbon cable
- Supports 1080p30, 720p60 and 640x480p90 video
- Small dimensions (24mm x 25mm x 9mm)

Part# (and link): Arducam B0470 camera (MSRP = $19.99)

14.4 MCU-LINK Debugger/Programmer Probe *(optional for M33 debug)*

The NXP MCU-LINK Debugger Probe configured for CMSIS-DAP protocol, is supported by multiple IDEs and is available for purchase separately from Avnet

Standard MCU-Link features:

- High speed USB,
- SWD debug,
- SWO profiling,
- VCOM (USB to UART bridge)

Part# (and link):MCU-LINK (MSRP = $10.99)

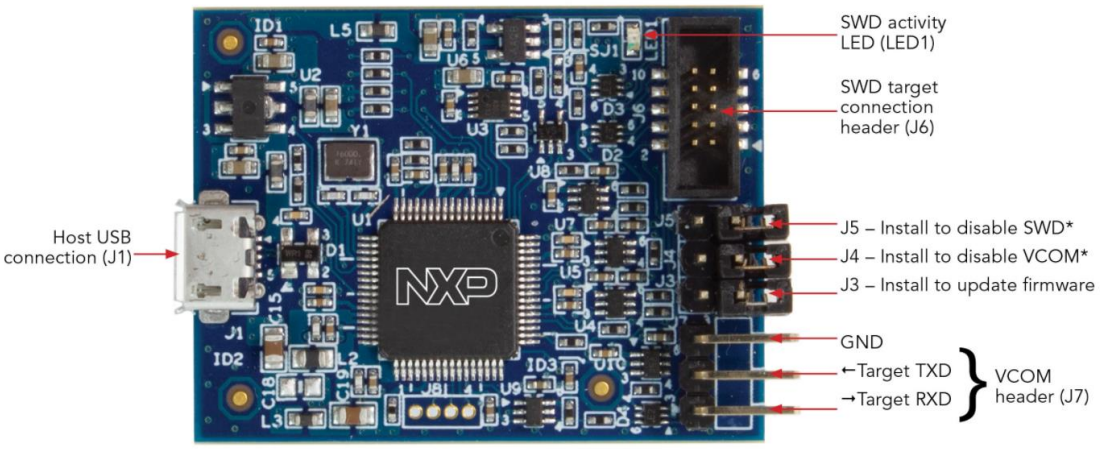


Figure 9 – NXP MCU-LINK Debug/Programmer Probe

14.5 MCU-LINK-PRO Debugger/Programmer Probe *(optional for M33 debug)*

The NXP MCU-LINK-PRO Debugger Probe alternative debugger probe has several enhancements

Features in common with MCU-Link:

- High speed USB
- SWD debug
- SWO profiling
- VCOM (USB to UART bridge)

Advanced MCU-Link-Pro features:

- Target energy/power measurement
- USB SPI & I2C bridges for programming/provisioning & host-based application development
- On-board, user-programmable LPC804 for peripheral emulation
- SEGGER J-Link firmware option
- Option to power target system (at 1.8V or 3.3V)
- Hardware capabilities for future enhancements

Part# (and link):MCU-LINK-PRO (MSRP = $39.99)

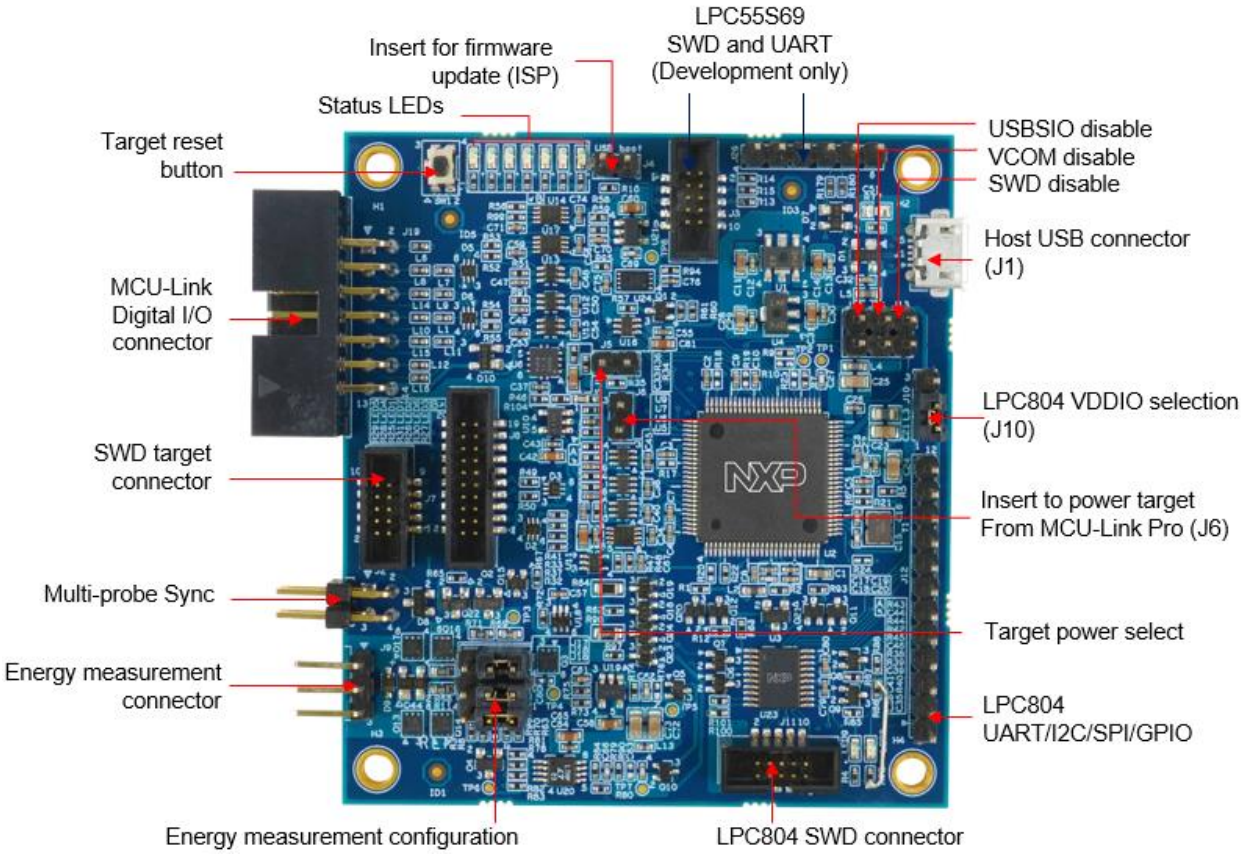


Figure 10 – NXP MCU-LINK-PRO Debug/Programmer Probe

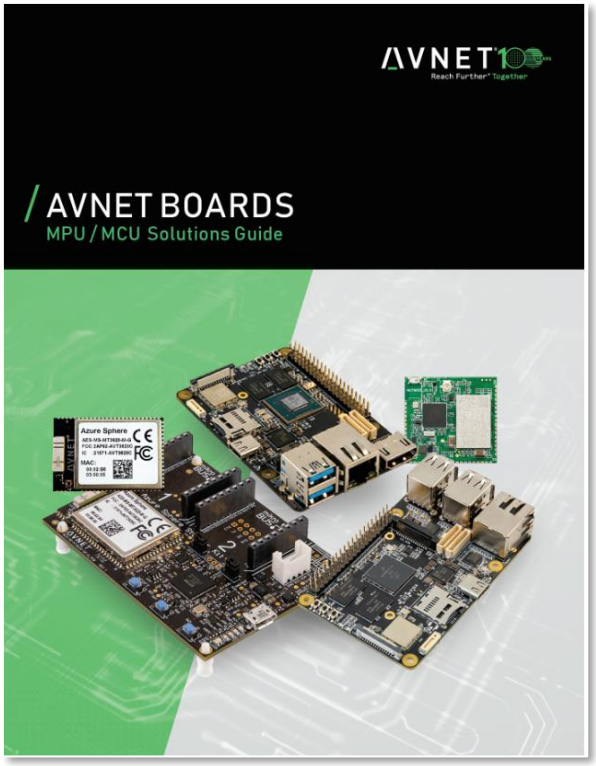
14.6 Other SBCs, SOMs and Accessories from Avnet Boards

Avnet's **Advanced Applications Group** work in close partnership with key suppliers to develop advanced enablement solutions

- Kits / Boards / SOMs / Modules
- Reference Designs
- Trainings / Tutorials / Blogs

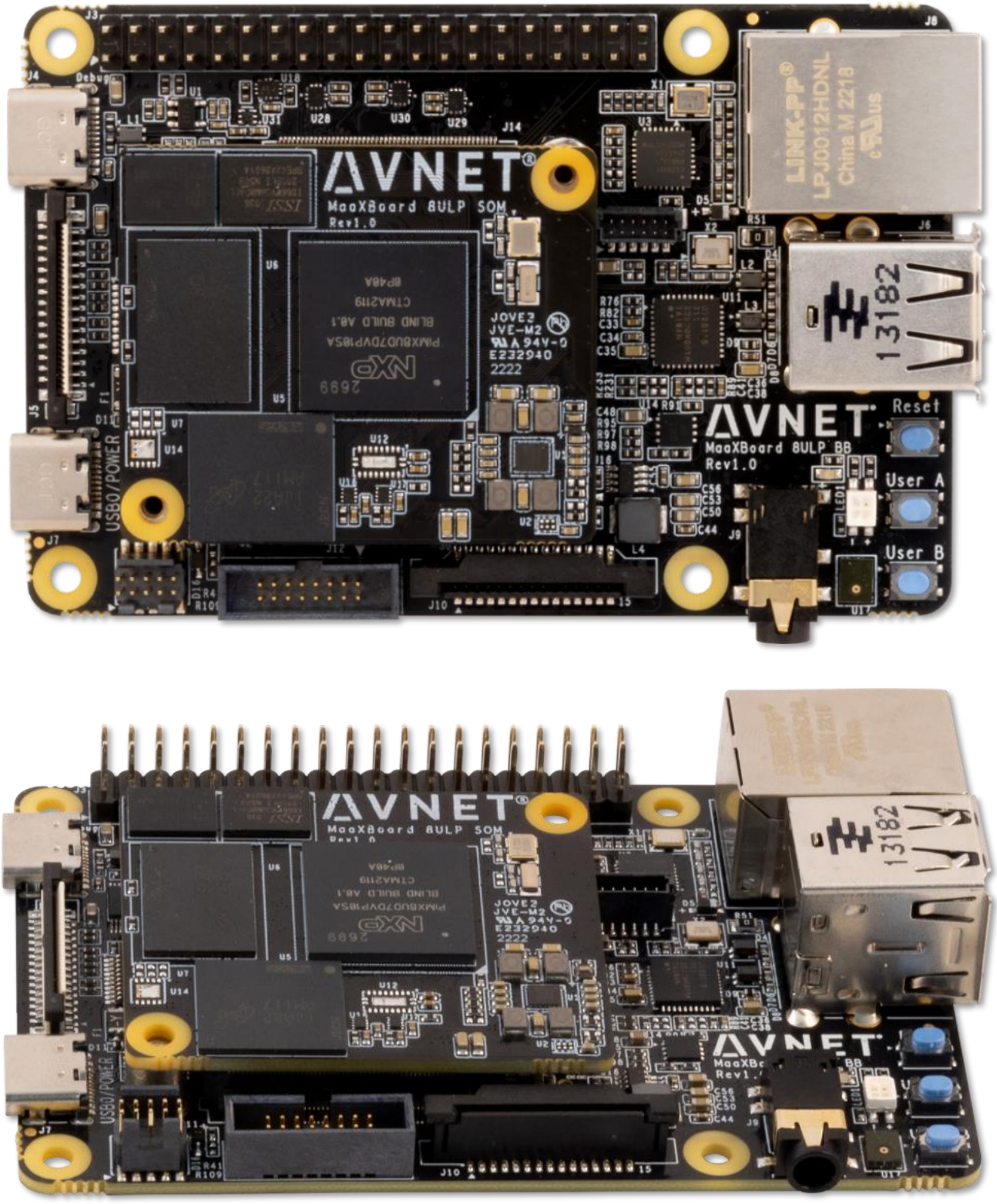
For more information, visit avnet.me/avnetboards

Downloadable **Solutions Guides** are also available:



https://avnet.me/mpu-mcu-solutions-guide-2022

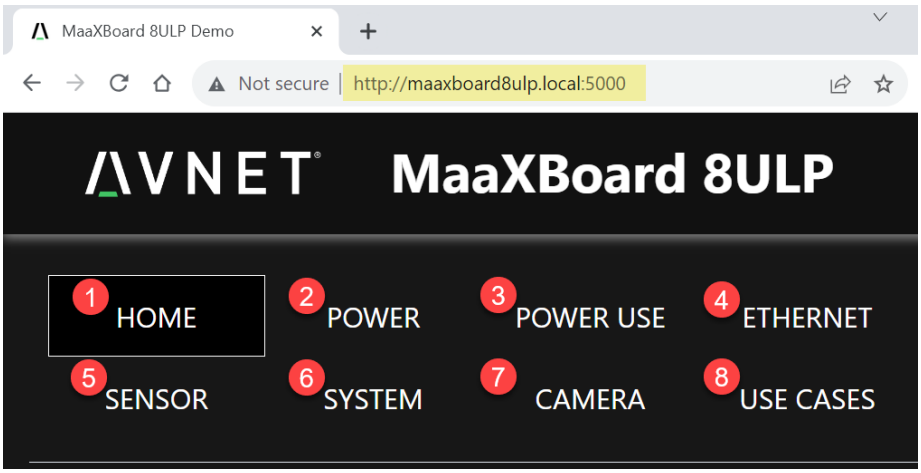
https://avnet.me/xlx-solutions-guide-2022


AVNET
MaaXBoard 8ULP SOM
Rev1.0
AVNET
MaaXBoard 8ULP BB
Rev1.0
Reset
User A
User B
USB0/POWER
LINK-PP
LPJ0012HDNL
13182

15 MaaXBoard 8ULP Out-of-Box Demo Application

The Out-of-Box webserver demo application auto-starts after power-up of the board

Multiple webpages are available for access via eight menu tabs…



1) **Home** - MaaXBoard 8ULP info page

2) **Power** - Live monitoring of supply current (*requires TC66 power measurement USB dongle)
RGB LEDs can be manually controlled and
Display PWM backlight power can be adjusted via onscreen slider widget

3) **Power Use** - Analysis of where the measured power is being used

4) **Ethernet** - Live reporting of Ethernet interface session information

5) **Sensor** - 6-axis IMU sensor and proximity sensor (animated simulation)

6) **System** - Live reporting of system resource utilization

7) **Camera** - Live video from MIPI-CSI camera

8) **Use cases** - Simulated real world applications, as well as add-on demo options, e.g.
Camera based badge-scan security access-control demo (with AWS/Azure dashboard)

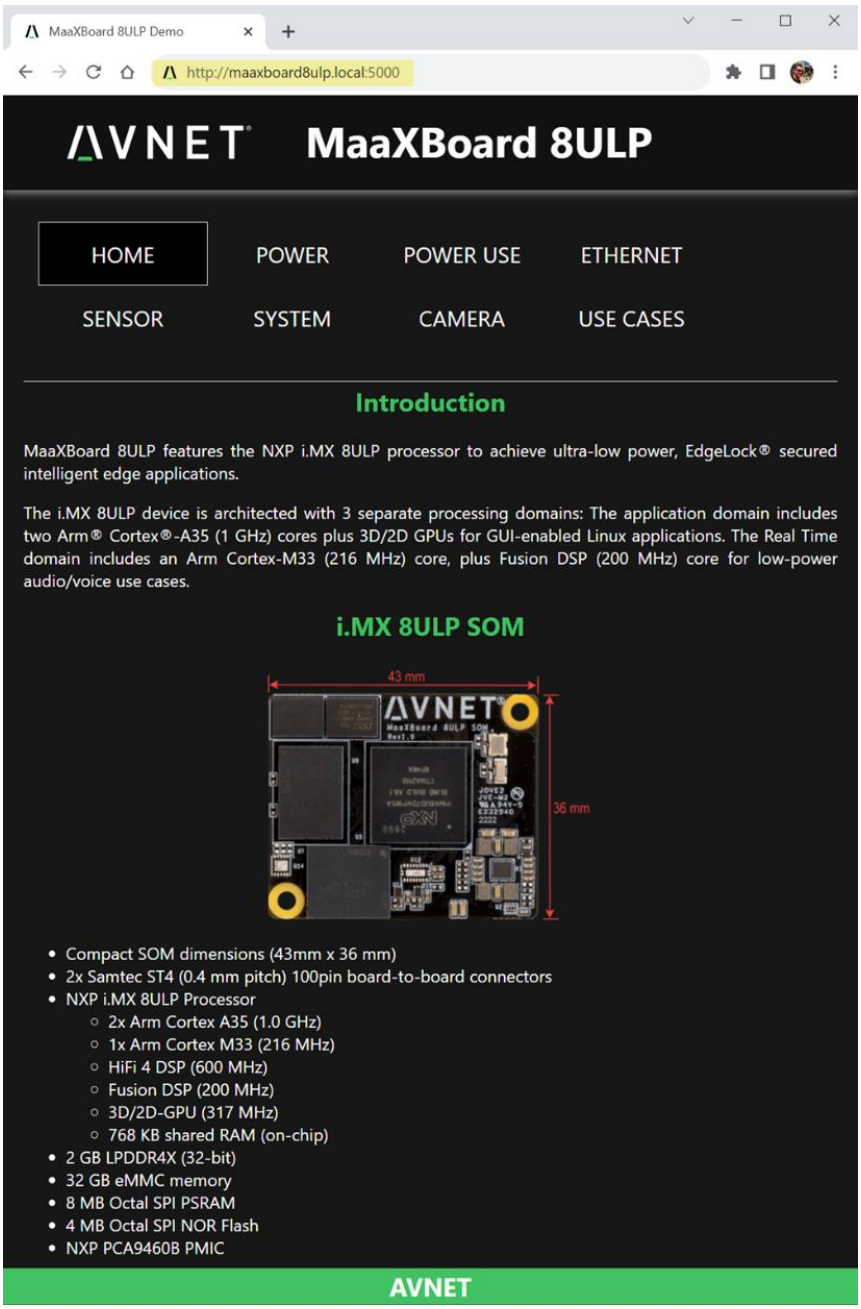
Standalone - In the most minimal configuration (just MaaXBoard 8ULP without accessories), a subset of the available functions can be exercised from an Internet Browser on the development PC

+Accessories – Adding a CSI camera, touchscreen and power measurement dongle provides a fuller experience, where a Chromium browser provides local access via the MIPI touchscreen and live power measurement figures are reported and analyzed.

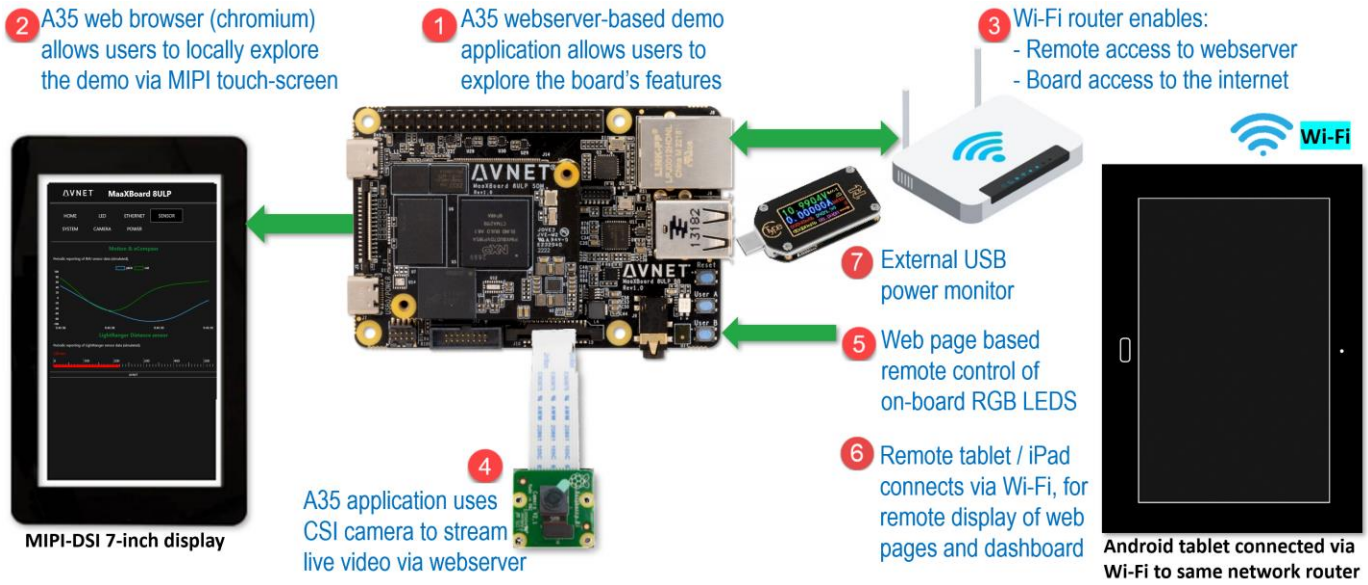
+iPad/Android tablet – By connecting the Ethernet port to a network router rather than directly to the PC, tablet or smartphone access to the webserver can be exercised.

The simplest / minimum hardware setup needed to access webserver pages from your board is as follows:

1) Connect MaaXBoard 8ULP via Ethernet to the same network router that your PC is connected to.
2) Power-up the board by connecting 5V (from host PC or a power adapter) to the lower USB-C connector
3) Open an Internet browser on the host PC and enter the following address: http://maaxboard8ulp.local:5000/
4) The following webpage should now display in the browser…



More comprehensive exercises are possible when MaaXBoard 8ULP accessories are added…
(ie. MIPI camera, MIPI display and current measurement USB dongle)



<u>Method without using network router</u>:
If connecting MaaXBoard 8ULP directly via Ethernet with the host computer, rather than through a shared network router, - in this case some additional steps will be needed.

The host PC and board must be configured with IP addresses on same sub-LAN,
eg. both have an address in same range like this **`192.168.1.xx`**

To achieve this, a static IP address needs to be assigned to the PC's Ethernet adapter and the board's Ethernet address needs to be manually assigned using the following steps:

1) Connect a USB-C to USB cable from the lower USB-C connector to the host PC.
   Note the four new COM port numbers that enumerate on the host PC.

2) Open Tera Term, select 2nd highest COM port number that enumerated and configure it's settings for **1152008N1**

3) Connect an Ethernet cable between MaaXBoard 8ULP and the Ethernet interface of your host PC

4) Power-up the board. After booting completed, login as **`root`** at the commandline interface, then set the IP address of the MaaXBoard 8ULP Ethernet port to be on same sub-LAN network as the static IP settings of Ethernet adapter on the host PC. ie. Use this CLI command to set the **`eth0`** IP address:
   `ifconfig eth0 192.168.1.99`

   The host PC and board should have IP addresses on same sub-LAN, similar to what shown here:
   PC Ethernet IP address = **`192.168.1.88`**
   8ULP Ethernet IP address = **`192.168.1.99`**

5) Now view the webserver output by pointing your browser to the following address:
   http://maaxboard8ulp.local:5000 // (or use the board's IP address suffixed with port 5000)
   http://192.168.1.99:5000