New demands on DC link power capacitors

Congress on Automotive Electronic Systems - 3rd and 4th December 2014

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Abstract- **Due to the continuous development of power electronics following the trends of miniaturisation, increase of reliability, and improvement of efficiency, concrete demands on electronic components are claimed. Since new technologies and materials for semiconductors were successful introduced in the market in the last years, an improvement of passive components is mandatory as well. This paper introduces a new robust capacitor technology overcoming limits in the high temperature range and power density. Unique device features and characteristics will be explained enabling new ideas in power electronic designs. Furthermore, low inductive design solutions are discussed and an outlook for further developments is given.**

Keywords: CeraLink™, DC link capacitor, snubber, fast switching, antiferroelectric, high temperature, high frequency, low inductance, power modules, converter, inverter

1. Introduction

1.1 Trends in power electronics

Following the trends in power electronics both automotive and industry applications need compact, reliable and cost effective components to reach the major targets increased power density and miniaturisation. Key technologies like fast switching semiconductors are already successful used in the market today.

Since electronic components and its characteristics become more and more complex, design solutions have to be found on system level and in addition, the interaction of active and passive devices needs to be understood in detail. Especially during semiconductor switching, the DC link capacitor as part of the commutation loop has a lasting effect on the behavior and efficiency of the application. Different power electronic designs use low inductive assemblies of semiconductors and DC link capacitors to lower the voltage overshoot during turn-off [4]. In most cases, system designers have to deal with capacitors of big volume and large commutation loops. The new CeraLink™ capacitor technology, which is described in this paper and was introduced earlier in [1] and [2], shows high capacitance density as well as a very low self-inductance to keep the commutation loop inductance as low as possible.

1.2 DC link capacitors in power electronics

DC link capacitors are used in most power converters to stabilize the DC link voltage by balancing the interim difference between the input source and the output load. The voltage ripple needs to be minimized to avoid electrical stress to the source and semiconductors as well as to comply with EMI requirements. Furthermore, it acts as energy storage during the hold-up time. Beneath its major function, a DC link capacitor is requested to allow fast and efficient switching of the semiconductor by minimizing the necessary space.

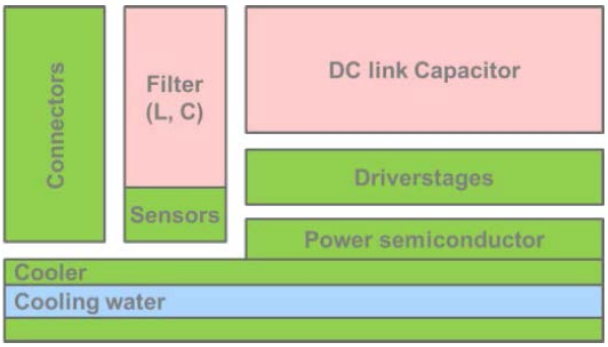


Figure 1 - principle block picture and size comparison of a motor inverter (source: Volkswagen AG [3])

To a large extent, the package of a motor inverter is driven by the DC link capacitor size [3]. Therefore high capacitance density is a major key parameter to decrease the inverter volume and to increase the power density. Together with a high current handling capability, a low self-inductance and an optimized connection technique, a compact DC link should be achieved. This principle is also true for other power electronic converters, where a miniaturisation of the DC link capacitor is needed. Additionally, robustness requirements must be fulfilled for defined stresses (thermal, electric, environmental, and mechanical).
Therefore, new developments in DC link capacitor technologies have to focus on the demands of next generations of power electronics.

2. Device characteristics

2.1 Ceramic material

The new CeraLink™ capacitor technology contains a lead lanthanum zirconate titanate ceramic (PLZT) as dielectric material ([1], [2]). Due to the fact, that the ceramic formulation is tuned to the anti-ferroelectric state, the capacitance is increasing with voltage and offers its highest capacitance values at DC-bus voltage levels. This overcomes the effect of a decreasing capacitance value known from ferroelectric class 2 ceramic materials used for MLCCs and improves therefore capacitance density at operating voltage levels.
Furthermore, the equivalent series resistance (ESR) decreases with frequency and temperature which allows efficient operation at high temperatures up to 150°C and high switching frequencies up to several MHz.

2.2 Electrode material

The material and design of the inner electrodes has a high impact on the performance of the capacitor, since electrical and thermal conductivity are directly related to the material properties and the arrangement inside the capacitor. Therefore copper was chosen as inner electrode material, providing excellent material properties.
Since new developments in power electronics tend to become more compact and efficient, the frequency, the current and the operating temperatures rise. Any additional self-heating of the capacitor and its connection needs to be prevented. Therefore all the materials serve the purpose of minimizing electrical resistivity in a preferably wide range of temperature and frequency.

2.3 Thermal conductivity

The device temperature of a capacitor is an important parameter for lifetime prediction and definition of the maximum permissible current. As the device temperature depends on the ESR and the ripple current, the heat that is produced by losses should be conducted from the capacitor as efficient as possible. Therefore the thermal resistance of a capacitor is an important characteristic.
In a steady state of operation, the capacitor's temperature is constant, the heat power produced by resistive losses (P_{loss}) equals the heat that is conducted from the capacitor (P_{th}).

$$P_{loss} = P_{th} \tag{1}$$

P_{loss} is calculated from the product of the sum of the ESR and the square of the ripple current $I_{C,rms}$ flowing through the capacitor. The heat is given by the right term of equation (2), where λ_{th} is the thermal resistance of the module, ΔT is the temperature difference, V the Volume of the device and l describes the length, along which the heat has to be conducted:

$$I_{C,rms}^2 \cdot ESR = \frac{\lambda_{th} \cdot \Delta T}{l^2} \cdot V \tag{2}$$

Writing the ripple current $I_{c,rms}$ explicitly (3), it can easily be seen that the ampacity is indirectly proportional to the length, where the heat has to be conducted. Apart from the capacitor size itself, which is mainly technology dependent, the increase of thermal conductivity, a low ESR and high permissible temperatures support the high current capability.

$$I_{C,rms} = \frac{1}{l}\sqrt{\frac{\lambda_{th} \cdot \Delta T \cdot V}{ESR}} \tag{3}$$

Regarding thermal conductivity, CeraLink™ technology offers the features mentioned above:

- a compact low profile design with short electric and thermal conduction paths l
- a high thermal conductivity λ_{th}
- a high permissible temperature increase ΔT
- low equivalent series resistance ESR

2.4 Performance

2.4.1 Current rating

Benefiting from the low losses and the high thermal conductivity of the CeraLink™ technology, high current ratings can be achieved.

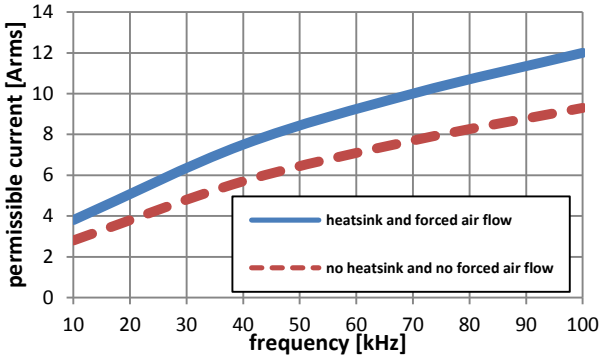


Figure 2 - typical permissible current depending on the cooling condition (ambient temperature 85 °C, measurement of 1 µF 500 V device), the permissible current corresponds to a device temperature of 125 °C

As one can see in Figure 2, a further increase of permissible current of approximately 25% can be reached at 100 kHz with simple forced cooling. Even with no heat sink and without any forced air flow

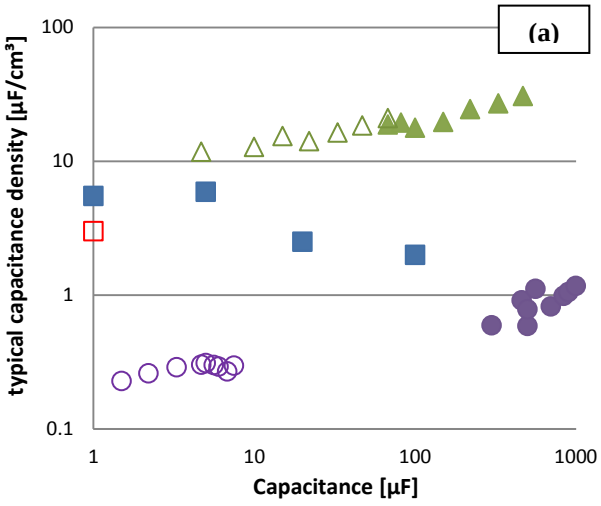
across the capacitor, high current ratings can be reached. A state-of-the-art power electronic PCB already provides sufficient thermal conductivity to operate the capacitor at high ripple currents.
Due to its design, larger assemblies of CeraLink™ ceramic chips (>1 µF) profit from the high thermal conductivity of the whole module too. Therefore high current ratings of more than 1 A/µF can be realized also for larger configurations whereas other technologies suffer from worse thermal conductivity due to size and conduction path lengths as well as the choice of the involved materials. Benefiting from its high thermal conductivity and its low losses, the CeraLink™ technology is able to handle more current per capacitance than competing technologies.

2.4.2 Power density

Comparing capacitor technologies, different technical benefits can be illustrated regarding a DC link capacitor miniaturisation (Figure 3 (a) and (b)):

- Aluminium electrolytic capacitors offer a very high capacitance density which makes them a cost effective solution when no high current ratings per capacitance are needed.
- Film capacitors offer good current ratings but suffer from a low capacitance density. In terms of permissible ripple current per capacitor volume, film capacitors equal aluminium electrolytic capacitors.
- Ceramic capacitors are the only technology, which combine both high capacitance density and high current rating.
- CeraLink™ exceeds conventional ceramic capacitors in terms of capacitance density and permissible current per capacitor volume. Furthermore, larger assemblies of up to 100 ceramic chips are available to achieve high capacitances.

For CeraLink™, current ratings without forced cooling are used. For other technologies, data sheet values are used for the calculation.



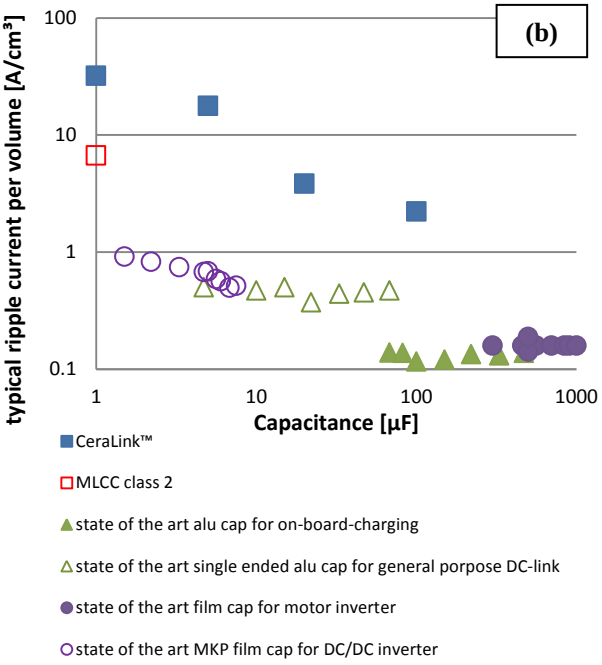


Figure 3 - comparison on capacitance per volume (a) and current per capacitor volume (b), please note, that the figures only account for capacitors with same voltage rating

2.4.3 Robustness at high temperatures

Another difference between capacitor technologies is thermal robustness. As a general rule, the leakage current of dielectric materials is increasing with temperature. A comparison of capacitor technologies can be seen in Figure 4. To compare different capacitance values, the time constant $\tau(T)$ was chosen (see equation 4), which corresponds to the self-discharging time constant of a capacitor. It calculates as the product of the insulation resistance at a given temperature $R_{ins}(T)$ and the capacitance value. By comparing this value, the different size and capacitance values of the capacitor technologies can be discarded, $\tau(T)$ is a size and voltage class corrected material constant.

$$\tau(T) = R_{ins}(T) \cdot C(T) \qquad (4)]$$

A low time constant corresponds to a high leakage current because it is proportional to the insulation resistance. For low time constants, the additional temperature increase due to the leakage current cannot be neglected and the risk of high temperature related failures like thermal runaway or avalanche breakdown is increased. CeraLink™'s time constant stays comparably high over a wide range of temperature, which enlarges the safety margin against temperature excursions. In contrast to other technologies, this would only reduce the lifetime of the capac-

itor, but does not lead necessarily to thermal runaway.

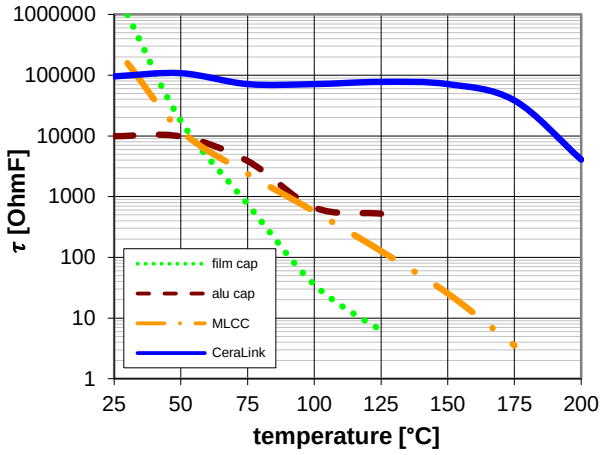


Figure 4 - insulation properties over temperature, capacitors with same voltage rating

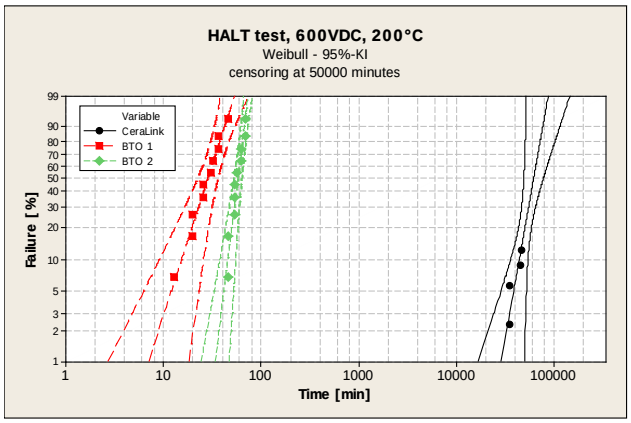


Figure 5 - lifetime at high temperatures

The most widely used model for lifetime prediction refers to the voltage (respectively electrical field) and temperature stress of capacitors and is well described in literature [5]. One test to determine the lifetime at steady state condition is a test with increased voltage and temperature levels. Comparing ceramic capacitors of the same capacitance, voltage, and temperature rating show an early breakdown for MLCC capacitors within tens of minutes. The test was stopped after 50.000 minutes when 4 samples out of 30 of the CeraLink™ material failed. The comparision can be seen in Figure 5 where CeraLink™ is compared with two different barium titanate oxide class 2 ceramic MLCC capacitors in a Weibull plot.

Regarding parallel connections of capacitors, the temperature dependency of the capacitance becomes relevant. As the impedance Z_n is inversely propotional to the current I_n through a capacitor, a parallel connection can be described as follows:

$$I_n = I_{tot}\frac{Z}{Z_n} \qquad (5)$$

$$\frac{1}{Z} = \sum_n \frac{1}{Z_n} \qquad (6)$$

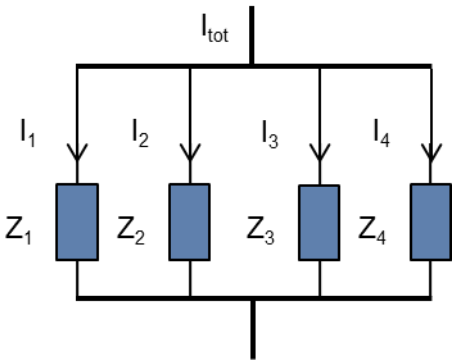


Figure 6 - Simple parallel connection of impedances

As one can see, the total current I_{tot} splits up between the capacitors. For temperature dependent capacitances a decrease of capacitance with temperature is crucial.

If this is not true, the capacitor with the highest temperature will have the highest capacitance which results in the lowest impedance Z_n and therefore the highest current I_n and the risk of a thermal runaway is increased. Figure 7 shows the capacitance characteristic of CeraLink™ with the small signal and large signal capacitance ([1], [2]). The small signal capacitance is measured with low ripple voltage signals of 0.5 V_{RMS}, whereas the large ripple signal capacitance is measured with high ripple signals of 20 V_{RMS}. As one can see, the capacitance is increasing with ripple voltage but this effect declines with temperature. High capacitance values are needed at low temperatures, especially at “cold start tests” known from automotive test programs.

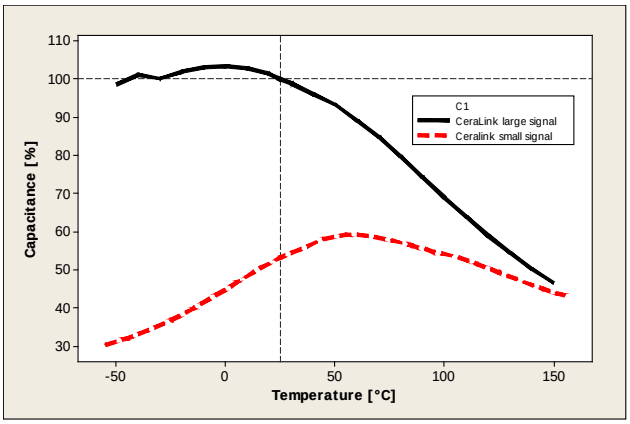


Figure 7 - Capacitance in dependence on temperature (V_{DC} = 400 V)

The negative capacitance characterisic at high temperatures is mandatory to minimize the risk of thermal runaway for the CeraLink™ material even when the rated temperature of 125 °C is clearly exceeded. When working in an array, the hottest capacitor faces the lowest current. This property

enables some sort of self regulating system, which makes CeraLink™ devices very stable against thermal gradients and the problems that can arise with that.

3. Device features

3.1 Product portfolio

Using a high-temperature stable ceramic-metal interconnection based on sinter silver, several assemblies can be realized. The basic unit is the ceramic chip which allows building up different modules. Different connection concepts are supported, especially the 20 µF device is available with both solder and press-fit pins. This devices allows also to be used in two pin configurations with 20 µF 500 V and 5 µF 1000 V.

The current product portfolio (Table 1) is optimized with the highest capacitance values for DC link voltages between 350 to 450 V_{DC} and therefore designed to be used with 600 to 650 V_{DC} rated semiconductors ([1], [2]). Following the trend of higher bus voltages the portfolio will be extended to the next voltage classes of semiconductors in the future.

3.2 Mechanical Robustness features

One of the most sensitive topics for ceramic capacitors is the mechanical and the thermo-mechanical stress and its relief during transport, mounting and operation. Classical failure modes for ceramic capacitors in SMD technology result from cracking of the ceramic material due to solder shock or mechanical overload due to bending of the PCB. This is the reason, why CeraLink™ is equipped with lead frames that are capable to reduce forces on the ceramic due to mechanical or temperature induced stress.

The outer termination of classical MLCCs is very often a metallic cap that provides a solderable connection to the exterior. The disadvantage of this caps is, that temperature shocks induced by soldering can cause cracks in the ceramic that start at the end of the cap going through the isolation zone into the active area of the ceramic. Therefore the cap was omitted in CeraLink™ capacitors. The outer electrode is solely connected on two opposing surfaces on the ceramic chip.

Additionally, another safety feature has been implemented into the CeraLink™ chip: the inner electrode arrangement forms a serial connection of the dielectric layers (multilayer serial ceramic capacitor design), which gives supplementary robustness against any failures in the active area. In contrast to the commonly known interdigital design of electrodes with opposing polarity, here is another set of electrodes acting as so called floating electrodes in the middle of the chip. The advantage of this arrangement is that even if there is a short occurring between two electrodes, the second part of the serial connection still acts as a capacitor and prohibits the flow of current.

The inner design of the ceramic layers also takes into account, that internal expansion caused by electrostrictive and piezoelectric forces in the active areas are compensated so, that even under highest field no mechanical damages can occur in the ceramic. The breakdown voltage of CeraLink™ devices is more than two times larger than their rated voltage which gives the system a lot of safety margin during operation.

4. Applications

4.1 General design parameters

To avoid a high voltage overshoot during fast semiconductor switching, a high ratio of DC link capacitance to commutation loop inductance is needed. In other words, a low self-inductance of the capacitor (E_{SL}) and a low stray-inductance caused by the connection (L_σ) combined with a high capacitance density is necessary (Figure 8). Furthermore, high temperature robustness allows CeraLink™ to be placed very close to the semiconductor. Following this assumption, a good connection between capacitor and semiconductor can be realized with low inductive designs [4], whereas integrating CeraLink™ into the semiconductor module shows the biggest benefit. First tests with embedded semiconductors and the capacitor directly mounted across the collector-emitter junction of the used bipolar transistors show lowest voltage overshoots.

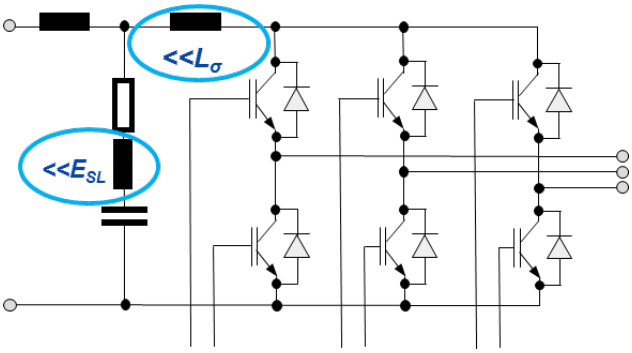


Figure 8 - commutation loop inductance with ideal semiconductors in a 3 phase configuration

4.2 Hybrid capacitor bank

Among minimizing the voltage ripple at the DC link, a certain amount of energy need to be stored in the capacitor for a well operating converter. As the needed capacitance value increases with decreasing

					
Rated capacitance [µF]	1	0.5	5	20 / 5	100
Rated voltage [V_{DC}]	500	700	500	500 / 1000	500
Self-inductance [nH]	2.5	2.5	3.5	3 / 6	6.6
Length, width, height [mm]	10.84 x 7.85 x 4.25	10.84 x 7.85 x 4.25	13.25 x 14.24 x 9.35	33 x 22 x 11.5	85 x 65.7 x 9.5

Table 1 – CeraLink™ product portfolio

switching frequency, bigger capacitance values might become necessary. Especially at higher power levels, the switching frequency cannot be increased due to efficiency and robustness reasons when using silicon semiconductors. This might change with the more frequent usage of wide-bandgap semiconductor switches and converter topologies with decentralized DC link capacitors where ceramic capacitors become cost effective for higher power levels in the application.

Today, converter designers consider hybrid capacitor banks to make use of the benefits of different capacitor technologies. For a 3.6 kW AC/DC PFC converter board for charger units CeraLink™ is used in parallel with an aluminium capacitor bank. This combination allows increasing the switching frequency up to 60 kHz which allows using smaller magnetic components. Due to the very low inductive high frequency commutation loop through the CeraLink™ capacitor, the voltage overshoot during switching is minimized since the high frequency part of the ripple current is now damped by CeraLink™. The aluminium capacitors can be moved farer away from the semiconductors to reduce the heat input which affects the lifetime positively.

Figure 9 - AC/DC PFC converter demonstrator (CeraLink™ in blue, 4 aluminium electrolytic capacitors in black)

5. Conclusion

Today's challenges in power electronics like higher power density, efficiency and reliability lead to new demands on DC link power capacitors. Higher capacitance densities combined with high current ratings and a high thermal robustness supports miniaturization and offers new solutions in power electronic design. Low inductive commutation loops allow improvement on the efficiency of semiconductor switching and become more important with the increasing usage of wide-bandgap semiconductors.
CeraLink™ already provides strongly enhanced features for facing these demands in today's high end systems and future applications. By targeting especially the demands named above via a module-based concept, that allows exceptional thermal stability and very low parasitic influences, CeraLink™ will emerge to be a key component in high efficient or ultra-compact DC link solutions of the future.

7. References

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